

Quantum using EcoStruxure™ Control Expert

140 EHC 105 00 High Speed Counter Module User Manual

(Original Document)

12/2018

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All pertinent state, regional, and local safety regulations must be observed when installing and using this product. For reasons of safety and to help ensure compliance with documented system data, only the manufacturer should perform repairs to components.

When devices are used for applications with technical safety requirements, the relevant instructions must be followed.

Failure to use Schneider Electric software or approved software with our hardware products may result in injury, harm, or improper operating results.

Failure to observe this information can result in injury or equipment damage.

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Safety Information



Important Information

NOTICE

Read these instructions carefully, and look at the equipment to become familiar with the device before trying to install, operate, service, or maintain it. The following special messages may appear throughout this documentation or on the equipment to warn of potential hazards or to call attention to information that clarifies or simplifies a procedure.



The addition of this symbol to a “Danger” or “Warning” safety label indicates that an electrical hazard exists which will result in personal injury if the instructions are not followed.



This is the safety alert symbol. It is used to alert you to potential personal injury hazards. Obey all safety messages that follow this symbol to avoid possible injury or death.

DANGER

DANGER indicates a hazardous situation which, if not avoided, **will result in** death or serious injury.

WARNING

WARNING indicates a hazardous situation which, if not avoided, **could result in** death or serious injury.

CAUTION

CAUTION indicates a hazardous situation which, if not avoided, **could result in** minor or moderate injury.

NOTICE

NOTICE is used to address practices not related to physical injury.

PLEASE NOTE

Electrical equipment should be installed, operated, serviced, and maintained only by qualified personnel. No responsibility is assumed by Schneider Electric for any consequences arising out of the use of this material.

A qualified person is one who has skills and knowledge related to the construction and operation of electrical equipment and its installation, and has received safety training to recognize and avoid the hazards involved.

BEFORE YOU BEGIN

Do not use this product on machinery lacking effective point-of-operation guarding. Lack of effective point-of-operation guarding on a machine can result in serious injury to the operator of that machine.

WARNING

UNGUARDED EQUIPMENT

- Do not use this software and related automation equipment on equipment which does not have point-of-operation protection.
- Do not reach into machinery during operation.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

This automation equipment and related software is used to control a variety of industrial processes. The type or model of automation equipment suitable for each application will vary depending on factors such as the control function required, degree of protection required, production methods, unusual conditions, government regulations, etc. In some applications, more than one processor may be required, as when backup redundancy is needed.

Only you, the user, machine builder or system integrator can be aware of all the conditions and factors present during setup, operation, and maintenance of the machine and, therefore, can determine the automation equipment and the related safeties and interlocks which can be properly used. When selecting automation and control equipment and related software for a particular application, you should refer to the applicable local and national standards and regulations. The National Safety Council's Accident Prevention Manual (nationally recognized in the United States of America) also provides much useful information.

In some applications, such as packaging machinery, additional operator protection such as point-of-operation guarding must be provided. This is necessary if the operator's hands and other parts of the body are free to enter the pinch points or other hazardous areas and serious injury can occur. Software products alone cannot protect an operator from injury. For this reason the software cannot be substituted for or take the place of point-of-operation protection.

Ensure that appropriate safeties and mechanical/electrical interlocks related to point-of-operation protection have been installed and are operational before placing the equipment into service. All interlocks and safeties related to point-of-operation protection must be coordinated with the related automation equipment and software programming.

NOTE: Coordination of safeties and mechanical/electrical interlocks for point-of-operation protection is outside the scope of the Function Block Library, System User Guide, or other implementation referenced in this documentation.

START-UP AND TEST

Before using electrical control and automation equipment for regular operation after installation, the system should be given a start-up test by qualified personnel to verify correct operation of the equipment. It is important that arrangements for such a check be made and that enough time is allowed to perform complete and satisfactory testing.

WARNING

EQUIPMENT OPERATION HAZARD

- Verify that all installation and set up procedures have been completed.
- Before operational tests are performed, remove all blocks or other temporary holding means used for shipment from all component devices.
- Remove tools, meters, and debris from equipment.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

Follow all start-up tests recommended in the equipment documentation. Store all equipment documentation for future references.

Software testing must be done in both simulated and real environments.

Verify that the completed system is free from all short circuits and temporary grounds that are not installed according to local regulations (according to the National Electrical Code in the U.S.A, for instance). If high-potential voltage testing is necessary, follow recommendations in equipment documentation to prevent accidental equipment damage.

Before energizing equipment:

- Remove tools, meters, and debris from equipment.
- Close the equipment enclosure door.
- Remove all temporary grounds from incoming power lines.
- Perform all start-up tests recommended by the manufacturer.

OPERATION AND ADJUSTMENTS

The following precautions are from the NEMA Standards Publication ICS 7.1-1995 (English version prevails):

- Regardless of the care exercised in the design and manufacture of equipment or in the selection and ratings of components, there are hazards that can be encountered if such equipment is improperly operated.
- It is sometimes possible to misadjust the equipment and thus produce unsatisfactory or unsafe operation. Always use the manufacturer's instructions as a guide for functional adjustments. Personnel who have access to these adjustments should be familiar with the equipment manufacturer's instructions and the machinery used with the electrical equipment.
- Only those operational adjustments actually required by the operator should be accessible to the operator. Access to other controls should be restricted to prevent unauthorized changes in operating characteristics.

About the Book



At a Glance

Document Scope

This documentation is to serve as an aid to fast counter configuration.

- The operational characteristics of the EHC 105
- The module configuration and parameterization
- The module description EHC 105
- The configuration examples
- The EHC 105 derived data types

Validity Note

This document is valid for EcoStruxure™ Control Expert 14.0 or later.

Related Documents

title of documentation	Reference number
EcoStruxure™ Control Expert, Program Languages and Structure, Reference Manual	35006144 (English), 35006145 (French), 35006146 (German), 35013361 (Italian), 35006147 (Spanish), 35013362 (Chinese)

You can download these technical publications and other technical information from our website at www.schneider-electric.com/en/download.

Part I

EHC 105 00 Functional Overview

Introduction

This part includes information about functionality of the High Speed Counter EHC 105 00 module.

What Is in This Part?

This part contains the following chapters:

Chapter	Chapter Name	Page
1	EHC 105 00 Introduction	15
2	Structural Description of EHC 105 00	19
3	Operational Characteristics of EHC 105 00	25
4	EHC 105 00 Counter Types and their Operating Modes	41
5	Monitoring and Start-Up	63

Chapter 1

EHC 105 00 Introduction

Overview

This chapter includes information about global functionality of the High Speed Counter EHC 105 00 module.

What Is in This Chapter?

This chapter contains the following topics:

Topic	Page
General User Characteristics for EHC 105 00	16
System Characteristics of EHC 105 00	17

General User Characteristics for EHC 105 00

User Characteristics

The user characteristics are presented below:

- The EHC 105 00 module is a high-speed counter module for the Modicon Quantum controller.
- The EHC 105 00 includes 5 independent counters.
- Each counter can be operated with either 5 or 24 VDC pulse input signals.
- The counters can be operated in the following operating modes:
 - Event counter, 32-bit, with four distinct operating modes
 - Differential counter, 32-bit, with two distinct operating modes
 - Repetitive counter, 16-bit
 - Rate counter, 32-bit, with two distinct operating modes
- Counting frequencies of up to 100 kHz can be monitored, depending upon cable length, transmitter type and voltage refer to *EHC 105 00 Hardware Specifics, page 83*.
- There are eight isolated, discrete inputs and eight isolated, discrete outputs (24 VDC level) available. These I/O points can be assigned to the various signals of the individual counters.

System Characteristics of EHC 105 00

System Characteristics

EHC 105 is characterized by the following features:

- Configuration information is transferred from the controller to the EHC 105 00 module only at controller start up or module hot swap.
- Data transfer of the set point and actual values is exchanged every scan cycle.
- The user program is processed in the controller.
- The EHC105 module functions asynchronously with the controller, allowing fast response and control.

NOTE: Certain parameter defaults are assigned at module start-up, which among other things, assign specific functions to the discrete inputs. (Refer to *Overview of I/O Signals*, [page 23](#)).

Chapter 2

Structural Description of EHC 105 00

Introduction

This chapter describes the hardware configuration and the structure of the EHC 105 00 module.

What Is in This Chapter?

This chapter contains the following topics:

Topic	Page
Hardware Configuration of EHC 105 00	20
Block Diagram of a Counter Channel	21
Overview of I/O Signals	23

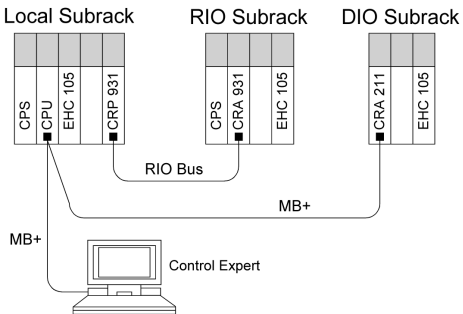
Hardware Configuration of EHC 105 00

Hardware Configuration

The counter module can be mounted in:

- Local subrack
- RIO subrack
- DIO subrack

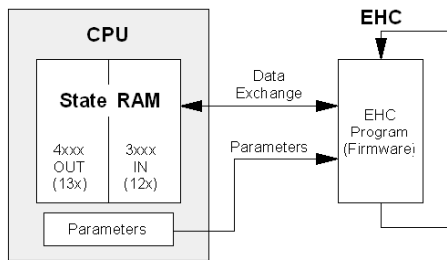
A typical hardware configuration is shown below.



State RAM Diagram

The counter module EHC 105 00 needs 13 OUT registers (4x...) and 12 IN registers for configuration.

The state RAM diagram as used by the counter is shown in the figure below.



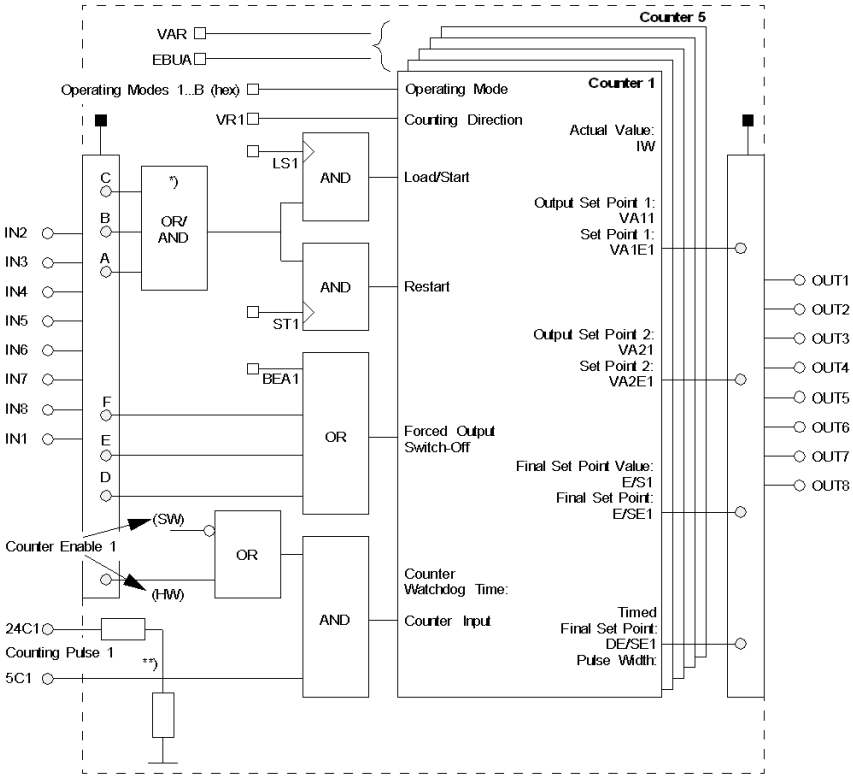
Block Diagram of a Counter Channel

Parts of a Counter Channel

Each counter channel consists of the following parts:

- Discrete input signals
- Input logic
- Input functionalities
- Output functionalities
- Output signals

Block Diagram



Symbols in the diagram:

Symbol	Meaning
*)	Configurable as either AND or OR. If the gate is not configured the output from this gate is TRUE.
**)	The counting pulse input voltage divider has been schematically simplified
○—	Discrete input signals
—○	Discrete output signals
□—	State RAM
—∩	Inversion
—	From Parameter configuration dialog
■ 	Discrete IN/OUT assignments to the internal counter signals and possible I/O inversions (through a configuration dialog)

Overview of I/O Signals

Signal	Description
IN1 ... 8:	Discrete input signals which can be connected and individually inverted to the counter's control inputs.
24Cx/5Cx (x = 1...5):	Discrete inputs for 24/5 VDC counting pulses.
VAR:	Bit within an output register (4x...), which determines if the output set points will be relative or absolute to final set point value for all 5 counters.
EBUA:	Output register (4x...) bit, which determines module switch-off behavior for all 5 counters when communication between the controller and EHC 105 00 is interrupted.
Operating modes 1...B:	One of 11 possible operating modes that can be selected for each counter through a 4x register.
VRx (x = 1...5):	Bit within an output register (4x...), which determines the counting direction.
LSx (x = 1...5):	Load/Start: Bit within an output register (4x...), minimum pulse width: 3 ms.
BEAx (x = 1...5):	Output switch-off: Bit within an output register (4x...). The pulse must be at least 3ms width.
STx (x = 1...5):	Counter restart: Bit within an output register (4x...), minimum pulse width: 3 ms.
Counter enablex:	There are two different enable inputs for every counter: <ul style="list-style-type: none"> ● Software Counter enable ● Hardware Counter enable
watchdog timer:	This timer monitors incoming pulses.
VA1x (x = 1...5):	The first output set point.
VA1Ex (x = 1...5):	First set point: Bit within an input register (3x...) to control the counter.
VA2x (x = 1...5):	Second output set point.
VA2Ex (x = 1...5):	Second set point: Bit within an input register (3x...) to control the counter.
E/Sx (x = 1...5):	Final set point value: Output register (4x...).
E/SEx (x = 1...5):	Final set point: Bit within an input register (3x...).
DE/SEx (x = 1...5):	Timed final set point: Settable through the parameter configuration screen.

Signal	Description
Pulse width:	Defines the length of the timed final set point pulse. In operating mode A: Defines the time for all associated outputs.
OUT1...8:	Discrete output signals, which can be assigned and individually inverted to the counter output.

Chapter 3

Operational Characteristics of EHC 105 00

Introduction

This chapter includes detailed information about the operational characteristics of the EHC 105 00 module.

What Is in This Chapter?

This chapter contains the following topics:

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Functional Counter Features	28
Start and Stop Counter Functionality	31
Start and Stop Priority Ranking of Signals	32
Start and Stop Timing Diagram without Hardware Input Configuration	33
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Counter Enabling and Monitoring	36
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Discrete I/O Signals

IN1...IN8

IN1 ... IN8 are discrete input signals which can be connected and individually inverted to the counter's control inputs

Response Times

The response times (including firmware scans) are:

- 10 ms for IN1...IN6
- 5 ms for IN7 and IN8

Rules

The following rules apply to IN1...IN8:

- Each INx signal may be selected several times.
- Every input may be assigned the load/start, restart, or forced output switch-off functions.
- Inputs can also be used as counter enable. However in this case the allocations are defined and may not be changed (IN1 is allocated counter 1, IN2 to counter 2, and so on.).
- Each discrete input can be inverted through the configuration dialogs.

Default

- The default for IN1...IN8 is **Not inverted**.
- For default assignment refer to *Start-Up Characteristics, page 67*.

24Cx/5Cx (x=1...5)

24Cx/5Cx (x = 1...5) are discrete inputs for 24/5 VDC counting pulses.

Counting on Pos. or Neg. Transition

Every counter has it's own counting pulse inputs.

You have the following choice for configuration of the counter:

If Input Signal counts on: ...	Then the counter will count on the ...
Is selected	Neg. Transition
Is not selected	Pos. Transition

The default is **Neg. Transition**.

OUT1...OUT8

OUT1 ... OUT8 are discrete output signals, which can be assigned and individually inverted to the counter outputs VA1E (set point 1), VA2E (set point 2), E/SE (final set point), and DE/SE (timed final set point).

Default

- The outputs OUT1...OUT8 are not inverted.
- The default assignment refer to *Start-Up Characteristics, page 67*.

WARNING

RISK OF UNPREDICTABLE PROCESS STATES

Do not select the same output OUT1 ... OUT8 with more than one set point.

Such double assignments lead to unpredictable process states, and are particularly difficult to diagnose.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

Functional Counter Features

Overview

The possible settings relating to the functional features of the five counters in your EHC 105 are described in the following. The figure below illustrates the setting possibilities.

Output Set Points

For all five counters the bit VAR determines if the output set points will be relative or absolute to final set point value. VAR is a bit within an output register (4x...).

The signal signification of VAR is:

- VAR = 1: output set point is relative (to the final set point value).
- VAR = 0: output set point is absolute.

Default setting for VAR before configuration is VAR = 0.

See also *Output Set Point Mode*, [page 38](#).

Module Switch-Off Behavior

The module switch-off behavior for all five counters when communication between the controller and EHC 105 00 is interrupted is determined by EBUA. EBUA is an output register (4x...) bit.

The signal signification of EBUA is:

- EBUA = 1: The current output state is retained.
- EBUA = 0: All used outputs are set to 0 level.

Operation Modes

The operation mode of each of the five counters is determined by the value of BA.

BA is a 4x register, which can take one of 11 values (1...9, A, B), each representing a specific operation mode. For the meaning of the values 1 ... B refer to *Counter Operating Mode Numbers*, [page 44](#).

Before configuration, the default mode of all counters is equivalent to operating mode A. The modes named 0, C, D, E, F are equal to the mode A.

Counting Direction

The individual counters can function as bidirectional counters, counting up or down.

The counting direction of each counter is determined by VRx (x = 1...5).

VRx (x = 1...5) is a bit within an output register (4x...).

The signal signification of VRx (x = 1...5) is:

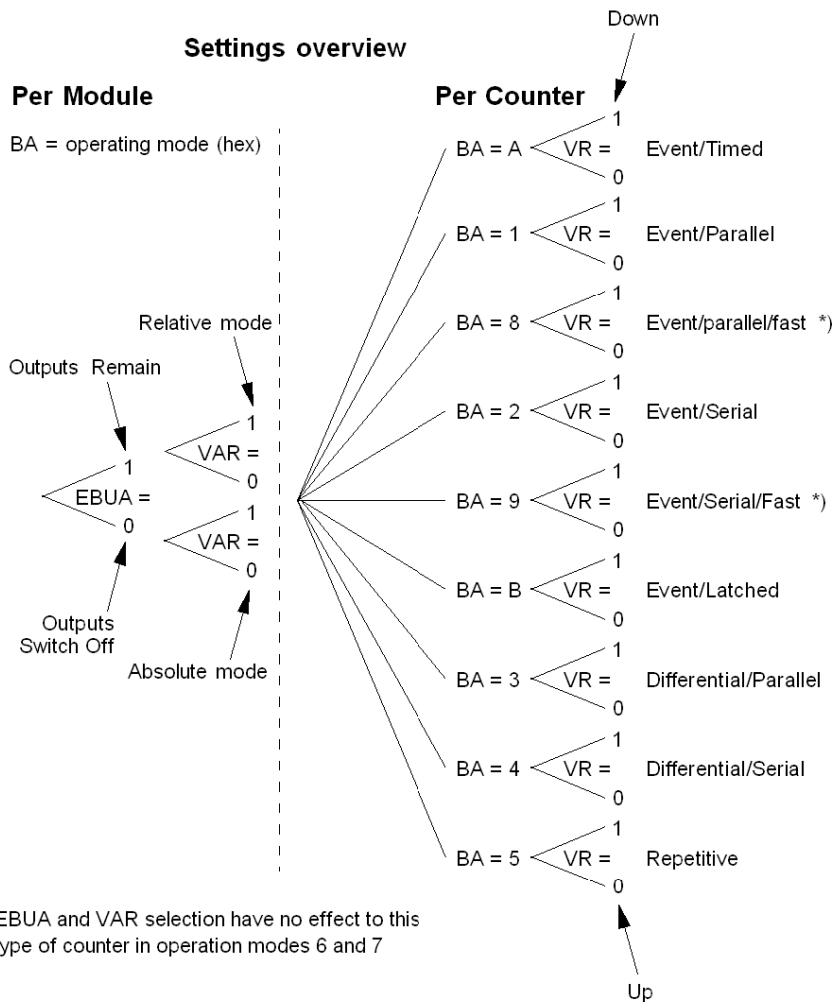
- VRx = 0: Up-counter, starting with 0, stop at final value E/Sx.
- VRx = 1: Down-counter, starting at initial value E/Sx, stop at 0.

NOTE: Do not change the value of the VRx bit during operation of the counter. If the value changes, the associated outputs of the counter will be switched off.

Before configuration, the default value for VRx is VRx (x = 1...5) = 0.

Counter Settings for Functional Features

Possible counter settings determining the functional features of the five counters are presented below:



EBUA and VAR selection have no effect to this type of counter in operation modes 6 and 7

BA = 6 VR = 0 Rate Counter 110 ms

BA = 7 VR = 0 Rate Counter 1 sec

*) Fast counters have no restart function

Start and Stop Counter Functionality

Load / Start

Load/start, LSx (x = 1...5), is a bit within an output register (4x...), minimum pulse width: 3 ms.

For more information refer to *Start and Stop Timing Diagram without Hardware Input Configuration*, [page 33](#) and *Start and Stop Timing Diagram with Hardware Input Configuration*, [page 34](#).

Default value before configuration is LSx (x = 1...5) = 0.

Output Switch-Off

Output switch-off, BEAx (x = 1...5), is a bit within an output register (4x...). The pulse must be at least 3 ms width.

If BEAx = 1, it latches the current count in a buffer. While the counter continues to count, VA1Ex, VA2Ex and E/SEx are reset. This is also true for any assigned outputs OUTx.

For more information refer to *Start and Stop Timing Diagram without Hardware Input Configuration*, [page 33](#) and *Start and Stop Timing Diagram with Hardware Input Configuration*, [page 34](#)

Default value before configuration is BEAx (x = 1...5) = 0.

Restart

Counter restart, STx (x = 1...5), is a bit within an output register (4x...), minimum pulse width: 3 ms.

The STx signal releases the buffer and counter values of equal current value.

For more information refer to *Start and Stop Timing Diagram without Hardware Input Configuration*, [page 33](#) and *Start and Stop Timing Diagram with Hardware Input Configuration*, [page 34](#)

Default value before configuration is STx (x = 1...5) = 0.

Start and Stop Priority Ranking of Signals

Priority Ranking

The priority of signals to start or stop a counter is as follows:

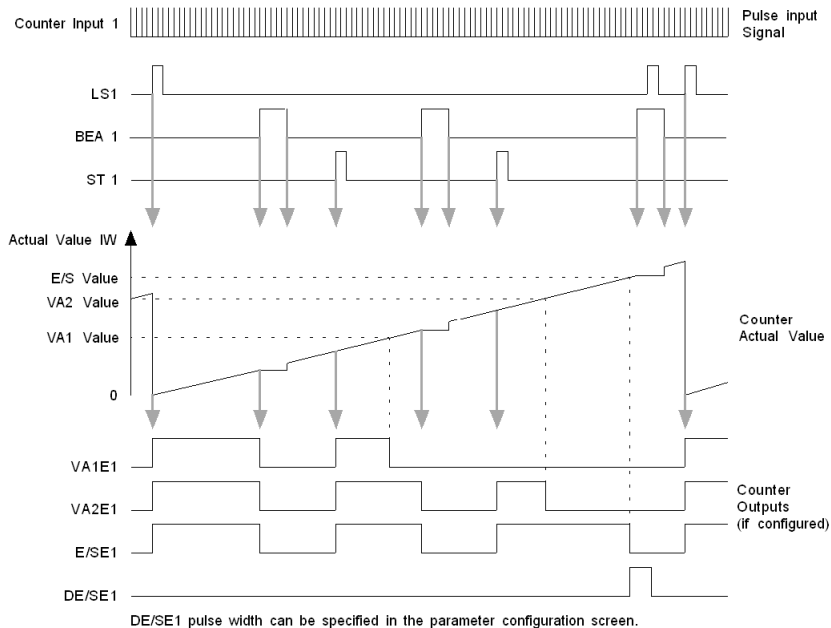
Priority	Function	Active for:
1	Forced output switch-off	BEAx = 1 (state RAM) or One of the configured discrete inputs is 1.
2	Load/Start counter	LSx = 1 (state RAM) and TRUE evaluation of the configured discrete inputs
3	Restart counter	STx = 1 (state RAM) and TRUE evaluation of the configured discrete inputs

NOTE: The user program commands are necessary for starting and restarting of the counting procedures. Setting of the corresponding discrete inputs is also required. When no discrete input is assigned to the commands through **Load/Start** and **Restart**, the counting procedure is initiated through the output status word (4x...) bits LSx respectively STx.

Start and Stop Timing Diagram without Hardware Input Configuration

Timing Diagram

The following timing diagram shows the start and stop functionality without using the input signals load/start, restart, output switch-off and counter enable. Counter 1 is configured as event counter, parallel, absolute, output function noninverted and counting up.



Influence of LS1

With the rising edge from LS1, the actual counting value is set to 0. The outputs VA1E1, VA2E1 and E/SE1 are set to 1 for the operation mode 1 ... 5 and 8, 9 or to 0 for operation mode A and B.

Influence of BEA1 and ST1

If BEA1 = 1 the actual value will latch; the counting continues in an internal memory of the module.

If BEA1 = 0 the counting of the actual value continues with the current contents of the memory. Is there on ST1 a rising edge the outputs switch on depending on the actual value.

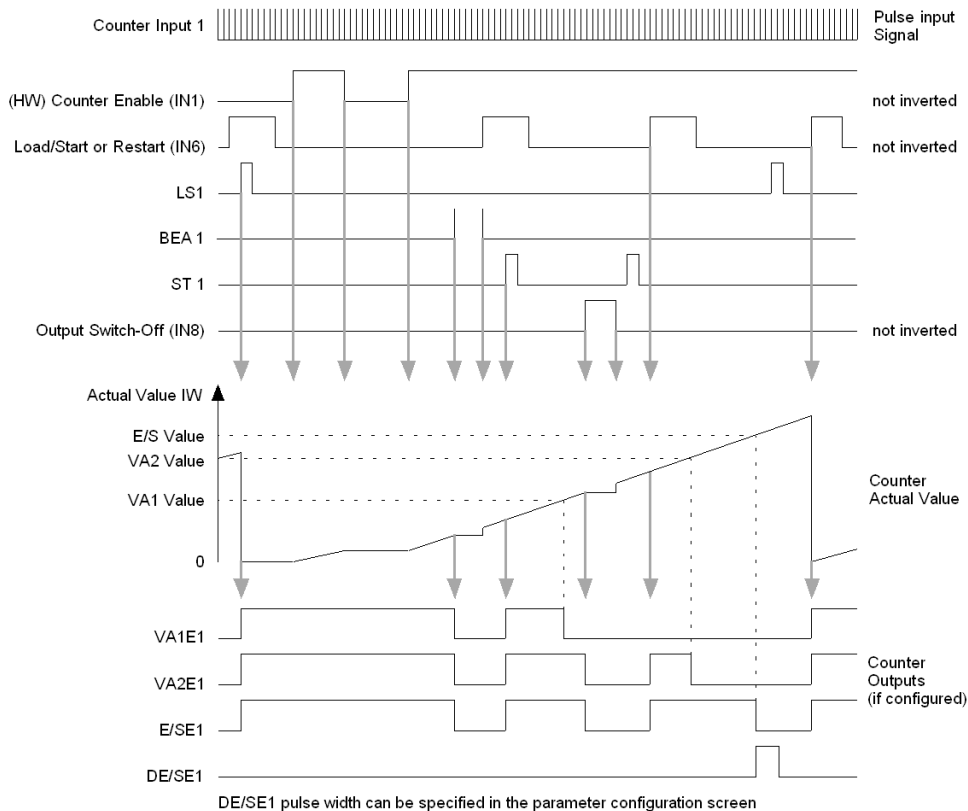
NOTE: Notice following notes:

- In mode 5, 8, 9 an 1 signal at BEA is setting the actual value to 0 or to final set point value, depending on up or down counting mode.
- The ST1 signal has no function in the modes 5, 8 and 9.

Start and Stop Timing Diagram with Hardware Input Configuration

Timing Diagram

The following timing diagram shows the start and stop functionality with using the input signals load/start, restart, output switch-off and counter enable. Counter 1 diagram as event counter, parallel, absolute, output function non inverted and counting up.



Load/Start or Restart

- The discrete input evaluation for **Load/Start or Restart** is combined with LSx respectively STx by AND.
- The AND condition is true if no configuration has been carried out for **Load/Start or Restart**; the LSx and STx bits then function alone.

Influence of LSx and STx

- The LSx and STx signals operate edge-controlled.
- LSx and STx bit are always active with the rising edge, it can not be inverted.

Influence of BEAx

- BEAx is always active with the high signal, it can not be inverted.
- An active BEAx signal set all inverted outputs to high signal.

Discrete I/O

- If the discrete outputs are inverted, the state from the signals VA1Ex, VA2Ex and E/SEx will not be inverted.
- If the discrete input is not inverted, the high signal is active. If discrete input is inverted, the low signal is active.

Output-Switch-Off

- The output switch-off discrete inputs have the same function as the BEAx bit.

Counter Enabling and Monitoring

SW Counter Enable 1-5

The software switch enables the counter and is activated from the parameter configuration screen. In the screen select the option as follows:

Option	Meaning
Input x for counter enable: is selected	The (HW) counter enable is effective.
Input x for counter enable: is not selected	The counting pulse is always enabled.

The default is **Input x for counter enable: is not selected**.

NOTE: The pulse counting begins after the first complete pulse following the counter enable signal. Accordingly, after counting pulse disable, the next counting pulse will still be registered. As a result during each count cycle (enable / disable), one pulse will be missing.

HW Counter Enable 1-5

Signal that enables the counter, if **Input x for counter enable** is selected. Input channels for this function are predefined:

Input	Counter
IN1	1
IN2	2
:	:

The signal signification for the (HW) counter enable is:

Signal	Meaning
1	Counter is enabled (input not inverted)
0	Counter is disabled (input not inverted)

The default: Input (HW counter) is not selectable for counter enable.

NOTE: The pulse counting begins after the first complete pulse following the counter enable signal. Accordingly, after counting pulse disable, the next counting pulse will still be registered. As a result during each count cycle (enable / disable), one pulse will be missing.

Counter Watchdog Timer

This timer monitors incoming pulses and can be enabled through the parameter configuration screen:

The parameter signification is:

- Value 0: no monitoring
- Values 1...255: (x 0.1) sec.

The default is value 0.

Output Set Point Mode

Output Set Points

There are two output set points per EHC module:

- The first output set point VA1x (x = 1...5)
- The second output set point VA2x (x = 1...5)

The output set point is configured once for all module counters. All counters of one module operate in absolute or relative output set point mode.

Value range of VA1x = 0...(2 exp31) - 1

The default is value 0.

Output Set Point Modes

Signification and requirements of the output set points modes relative and absolute:

Output set point mode	Description	Requirement
Absolute	In this mode, the value entered in the parameter configuration screen is the actual output set point.	E/Sx > VA2x >=VA1x >=0 E/Sx = final set point value
Relative	In this mode, the output set point is the difference between the set point value and the final set point value.	E/Sx > VA1x >=VA2x >=0 E/Sx = final set point value

Set Points

Set Points

There are two set points per counter:

- VA1Ex ($x = 1...5$)
- VA2E ($x = 1...5$)

VA1Ex and VAE2x are bits within an input register (3x..).

They may be assigned to any of the discrete outputs OUT1...OUT8.

Default: VA1Ex ($x = 1...5$) = 0 and VA2Ex ($x = 1...5$) = 0.

For default assignments refer to *Start-Up Characteristics, page 67*.

Final Set Point Value

The final set point value E/Sx ($x = 1...5$) is an output register (4x...) in which the counter's final value (up counter) or initial value (down counter) is entered.

A change of the final set point value has the following effects:

Mode	Effects
1, 2, 3, 4	A change of the final set point value will be excepted immediately (independent if the counter is active or inactive). The actual value will not be influenced.
5	A change of the final set point value only takes effect if the BEA signal is set in advance.
8, 9	A change of this value has no effect, if the counter is active. If the counter is inactive a change of this value is excepted immediately. The actual value is setting to 0 or to final set point value, depending on up or down counting mode.

Value range: E/Sx ($x = 1...5$) = $0...(2 \exp 31) - 1$

Default value: E/Sx ($x = 1...5$) = 0

Final Set Point

The final set point E/SEx ($x = 1...5$) is a bit within an input register (3x..).

It may be assigned through the parameter configuration screen to any of the discrete outputs OUT1...OUT8.

Default value: E/SEx ($x = 1...5$) = 0.

For default assignments refer to *Start-Up Characteristics, page 67*.

Timed Final Set Point

The timed final set point DE/SE_x ($x = 1...5$) is settable through the parameter configuration screen. It can be assigned to any of the discrete outputs OUT1...OUT8.

Default value: DE/SE_x ($x = 1...5$) = 0.

Default assignment is: No assignment.

Pulse Width

Pulse width defines the length of the timed final set point pulse. In addition, in operating mode A, pulse width defines the time for all associated outputs.

Significance of the pulse width value:

Pulse width value	Significance
0	Output for DE/SE _x is disabled.
1...255	$x = 0.02 \text{ sec}$

Default: Pulse width = 0.

NOTE: If pulse width = 0 in operating mode A there will be no outputs.

Chapter 4

EHC 105 00 Counter Types and their Operating Modes

Introduction

This chapter includes information about the different Counter types and their possible operating modes.

What Is in This Chapter?

This chapter contains the following sections:

Section	Topic	Page
4.1	Overview of Counter Types and their Mode Numbers	42
4.2	Event Counter	45
4.3	Differential Counter	52
4.4	Repetitive Counter	57
4.5	Rate Counter	60

Section 4.1

Overview of Counter Types and their Mode Numbers

Introduction

This section describes the counter types and their mode numbers.

What Is in This Section?

This section contains the following topics:

Topic	Page
Counter Types	43
Counter Operating Mode Numbers	44

Counter Types

Counter Types

The EHC 105 00 module can operate as the following counter types:

- Event counter (with and without fast final set point)
- Event counter with timed or latched outputs
- Differential counter (without fast final set point)
- Repetitive counter (with fast final set point)
- Rate counter

Counting Up and Down

The selection of the various counter types takes place through the operating mode selections in state RAM. Every counter type can count up and down. Output set point mode can be set to be relative (to the final set point value) or absolute.

Reason for Switch-off

For an active counter, any of the following changes triggers an output switch-off:

- Change of operating mode
- Change of counting direction
- Change of switch-off behavior
- Change of type of set point

NOTE: A change of the operating mode accompanied by load/start is not possible. The setting of the load / start bit after changing the operation mode must be done in the next scan cycle.

Discrete Output Signal Response Times

The response times for discrete output signals:

Set Point	Discrete output signal response time
Without fast final set point	Typical 3 ms
With fast final set point	Typical 0.5 ms

Counter Operating Mode Numbers

Value (hex)	Meaning
1	Event counter with parallel set point activations.
2	Event counter with serial set point activations.
3	Differential counter with parallel set point activations (only applies to counters 1 and 3, the set point and actual values of counters 2 resp. 4 are inactive).
4	Differential counter with serial set point activations (only applies to counters 1 and 3, the set point and actual values of counters 2 resp. 4 are inactive).
5	Repetitive counter
6	Rate counter, gate time $t = 100 \text{ ms}$
7	Rate counter, gate time $t = 1 \text{ s}$
8	Event counter with parallel set point activations and fast final set point.
9	Event counter with serial set point activations and fast final set point.
A (default)	Event counter with timed ON outputs, the pulse width setting holds for all employed outputs.
B	Event counter with latched set point outputs.
0, C, D, E, F	As operating mode A.

Section 4.2

Event Counter

Overview

This section describes the operating modes of EHC 105 00 when it is working as an event counter.

What Is in This Section?

This section contains the following topics:

Topic	Page
Operating Modes	46
Time Diagrams for Operating Modes 1 and 8	47
Time Diagram for Operating Modes 2 and 9	49
Time Diagram for Operating Mode A	50
Time Diagram for Operating Mode B	51

Operating Modes

Event Counter Characteristics

The event counter is a gate-controlled, bidirectional counter with two or fewer set points—a final set point and a timed final set point.

Operating Modes

Operating Mode	Description
A	With adjustable time-on outputs.
	The pulse width configuration applies the same value to all counter outputs.
1	With parallel output set point activation.
2	With serial output set point activation.
8	With parallel output set point activation and fast final set point.
9	With serial output set point activation and fast final set point.
B	With latched set point activation.

NOTE: Outputs are at 0 signal on start.

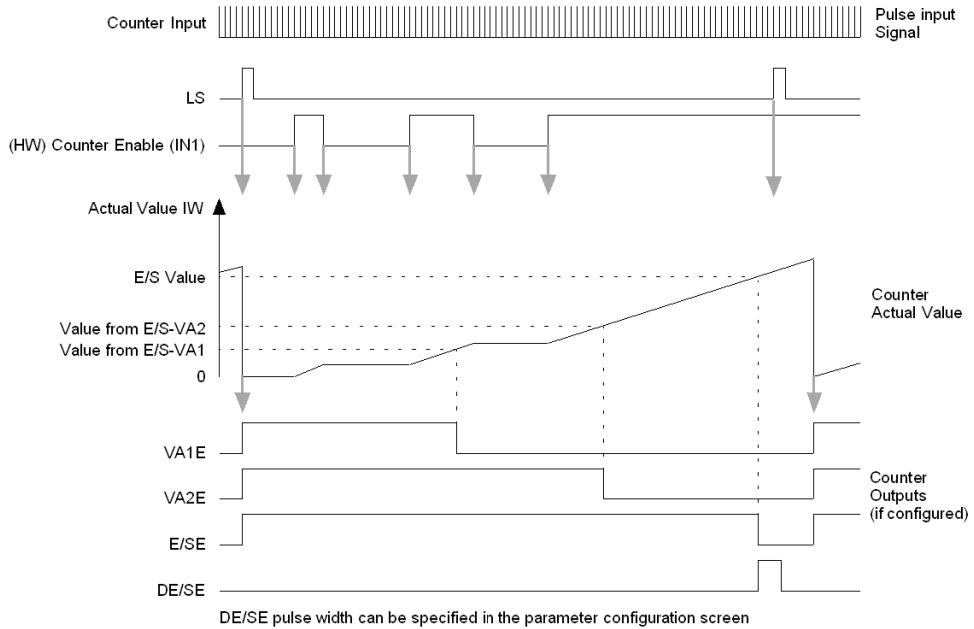
Value Range

The value range for all operating modes amounts to: $0 \dots (2^{\text{exp } 31}) - 1$, except the operating mode 5 is $0 \dots (2^{\text{exp } 16}) - 1$.

Time Diagrams for Operating Modes 1 and 8

Counting up

Counting up is realized with $VRx = 0$.



Further Signals

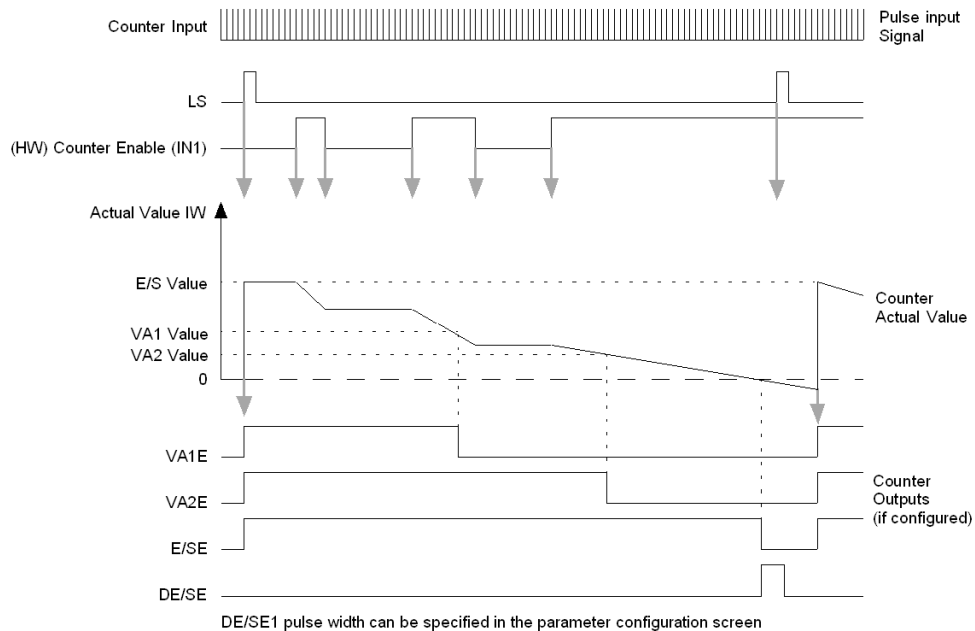
This is a typical time diagram of an event counter with relative and serial set point activation that does not take into account the following signals:

- BEAx (*see page 31*)
- STx (*see page 31*)

NOTE: STx has no function in the operating mode 8.

Counting down Counter

Counting down is realized with $VRx = 1$.



Further Signals

This is a typical time diagram of an event counter with relative and serial set point activation that does not take into account the following signals:

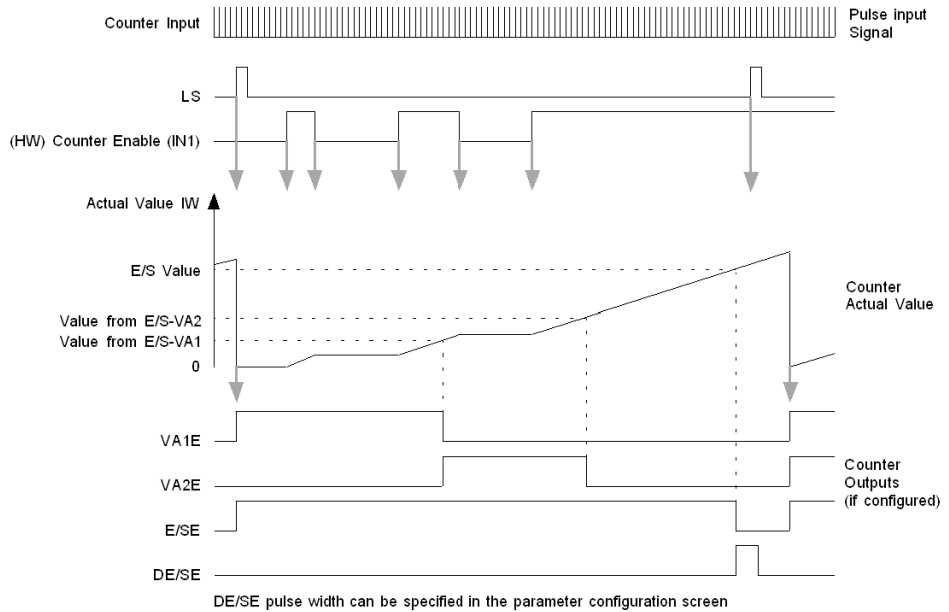
- BEAx
- STx

NOTE: STx has no function in the operating modes 8.

Time Diagram for Operating Modes 2 and 9

Counting up

Counting up is realized with $VRx = 0$.



Further Signals

This is a typical time diagram of an event counter with relative and serial set point activation that do not take into account the following signals:

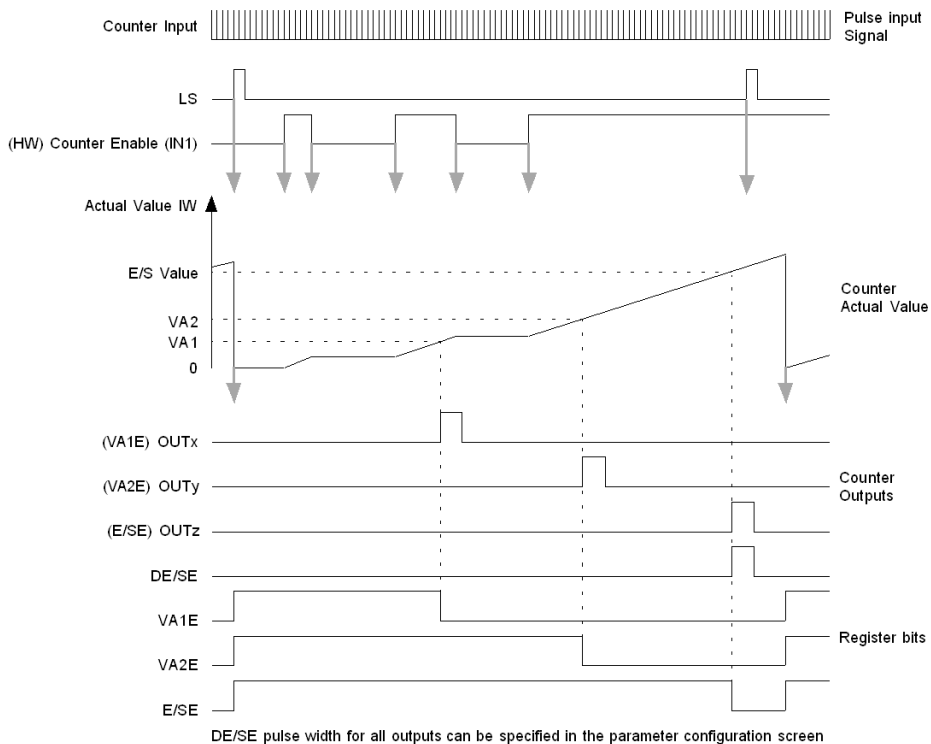
- BEAx (*see page 31*)
- STx (*see page 31*)

NOTE: STx has no function in the operating mode 9.

Time Diagram for Operating Mode A

Counting up

Counting up is realized with $VRx = 0$.

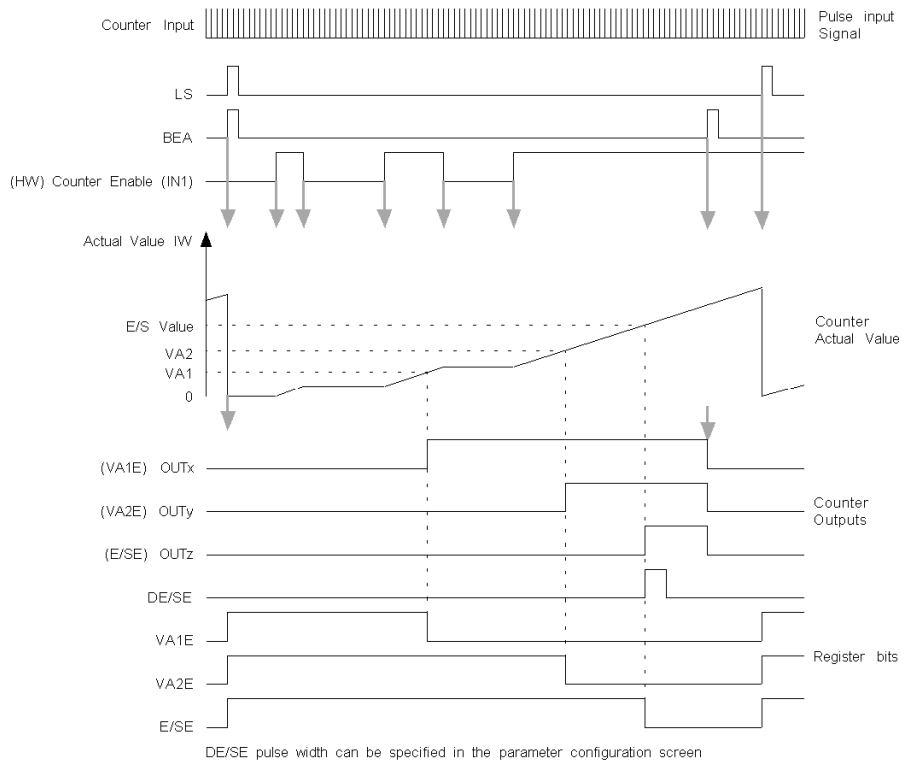


NOTE: The activation of the discrete outputs are different from the activation of the register bits.

Time Diagram for Operating Mode B

Counting up

Counting up is realized with $VRx = 0$.



NOTE: The activation of the discrete outputs are different from the activation of the register bits.

Section 4.3

Differential Counter

Introduction

This section describes the operating modes of EHC 105 when it is working as a differential counter.

What Is in This Section?

This section contains the following topics:

Topic	Page
Operating Modes	53
Time Diagram for Operating Mode 3	54
Time Diagram for Operating Mode 4	56

Operating Modes

Differential Counter Characteristics

The differential counter is a gate-controlled counter with up to two output set points, a final set point and a timed final set point. A differential counter consists of two counter channels and measures the difference between each of their pulses.

The counting value is determined from the difference between the two counters.

Counter 1 (clockwise) and 2 (counterclockwise) form a differential counter 1, while counter 3 (clockwise) and 4 (counterclockwise) form a differential counter 2.

NOTE: This configuration cannot be changed.

Operating Modes

The differential counter has the following operating modes:

Operating Mode	Description
3	With parallel set point activation.
4	With serial set point activation.

NOTE: Outputs are at 0 signal on start.

Configuration

Differential counter configuration, control, and evaluation are done through the parameters and values of the first counter with the exception of the counter input.

The configuration for the respective second counter must be performed separately. The parameter choices from the parameter configuration screen are:

- **Invert counter input (input signal counts on)**
- **Use input for counter enable**

NOTE: A fast final set point cannot be set for differential counters. If a counter is disabled, counter time monitoring is suspended.

Value Range

The value ranges are as follows:

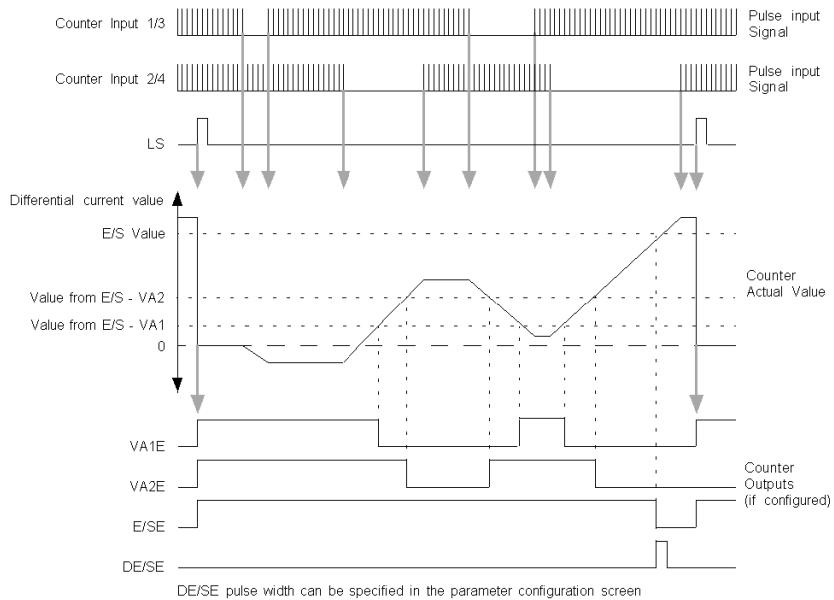
- Set Point values: $0 \dots (2 \exp 30) - 1$.
- Actual values: $-(2 \exp 30) \dots (2 \exp 30) - 1$.

NOTE: The value range allows the differential counter to be used also for continuous monitoring.

Time Diagram for Operating Mode 3

Counting up

Counting up is realised with $VRx = 0$.



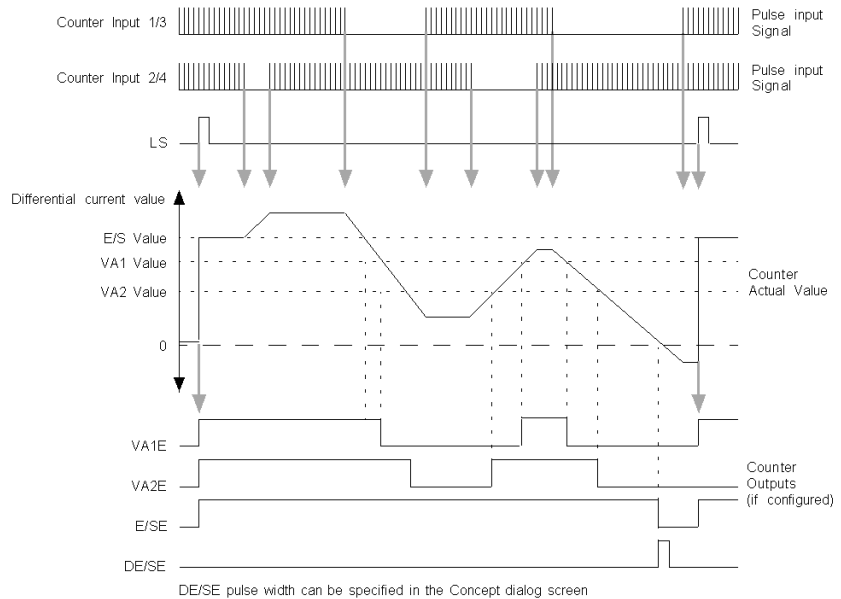
Further Signals

This is a typical time diagram of a differential counter with parallel set point cutoffs that does not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality, page 31*
- STx: Further information see *Start and Stop Counter Functionality, page 31*

Counting down

Counting down is realised with $VRx = 1$.



Further Signals

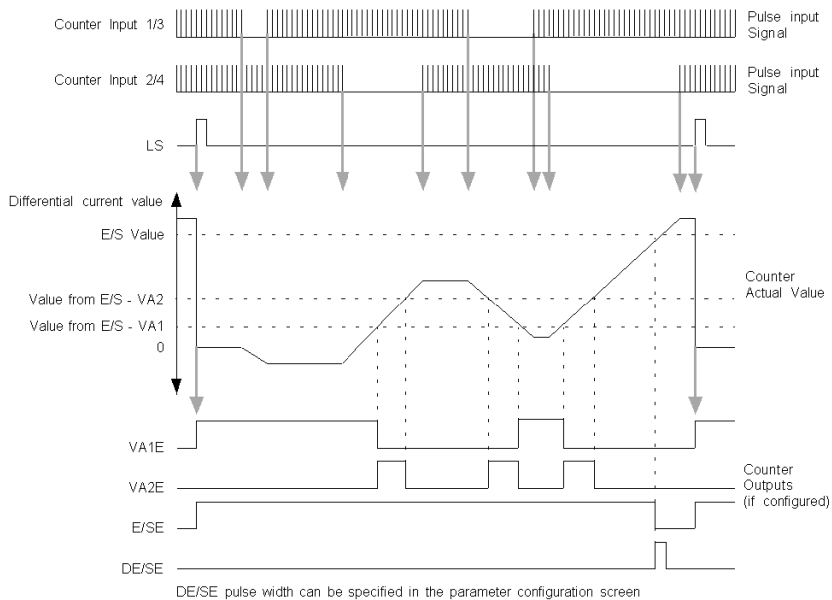
This is a typical time diagram of a differential counter with parallel set point cutoffs that does not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality*, page 31
- STx: Further information see *Start and Stop Counter Functionality*, page 31

Time Diagram for Operating Mode 4

Counting up

Counting up is realised with $VRx = 0$.



Further Signals

This is a typical time diagram of a differential counter with serial set point cutoffs that does not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality, page 31*
- STx: Further information see *Start and Stop Counter Functionality, page 31*

Section 4.4

Repetitive Counter

Introduction

This section describes the operating modes of EHC 105 if it is working as a repetitive counter.

What Is in This Section?

This section contains the following topics:

Topic	Page
Operating Mode 5	58
Time Diagram for Operating Mode 5	59

Operating Mode 5

Characterization

The repetitive counter is an up / down counter with up to two output set points, a fast final set point, which acts as a third set point and a timed final set point.

As a repetitive counter, every time the final set point value is reached, the following restrictions apply:

- E/Sx values are limited to the value ranges $0 \dots (2 \exp 16) - 1$.
- The final set point value cannot be changed when the counter is active. BEA must be set in advance.
- The final set point value must be equal or greater than 2.

Operating Mode

The repetitive counter has the following operating mode:

Operating Mode	Description
5	With serial output activation.

Synchronisation

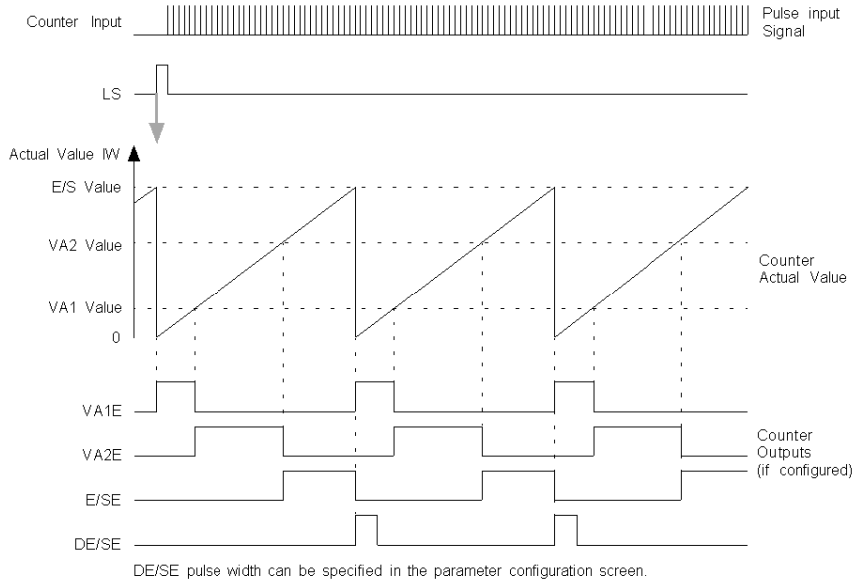
This enable / disable counter input is usable for synchronisation with an external event.

The next counting pulse after an edge 0->1 at the enable / disable counter input is setting the actual value to 0 or to final setpoint value, dependent from up or down counting mode.

Time Diagram for Operating Mode 5

Counting up

Counting up is realised with $VRx = 0$.



Further Signals

This is a typical time diagram of a repetitive counter that do not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality*, [page 31](#)
- STx has no effect in this operating mode.

Section 4.5

Rate Counter

Introduction

This section describes the operating modes of EHC 105 if it is working as a rate counter.

What Is in This Section?

This section contains the following topics:

Topic	Page
Operating Modes	61
Time Diagram for Operating Modes 6 and 7	62

Operating Modes

Characterization

The rate counter counts the number of pulses per unit time. A unit time is specified with the choice of the operating modes 6 or 7. The read value is then saved as the actual value.

The determined actual value thus represents the pulse count per unit time, and can be used to determine velocities, flow rates, or even revolutions.

Inputs and outputs are not processed in this counter type.

The watchdog timer function is not supported.

Operating Mode

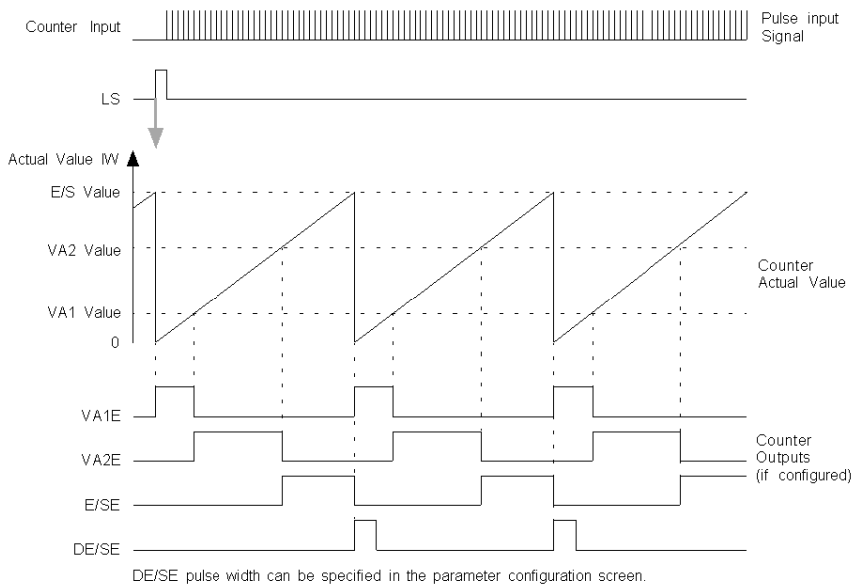
The rate counter has the following operating mode:

Operating Mode	Description
6	The gate time t amounts to 100 ms.
7	The gate time t amounts to 1 sec.

Time Diagram for Operating Modes 6 and 7

Counting up

Counting up is realised with $VRx = 0$.



Further Signals

This is a typical time diagram of a repetitive counter that does not take into account the following signals:

- BEAx: Further information see *Start and Stop Counter Functionality*, [page 31](#)
- STx has no effect in this operating mode.

Chapter 5

Monitoring and Start-Up

Introduction

This chapter includes information about monitoring and start up of the EHC 105 00 module.

What Is in This Chapter?

This chapter contains the following topics:

Topic	Page
Monitoring Incoming Pulses	64
Quantum System Bus Monitoring	65
US24 Monitoring	66
Start-Up Characteristics	67

Monitoring Incoming Pulses

Input Monitoring Function

The EHC 105 00 can monitor the presence or absence of incoming pulses.

If a pulse is not detected at the respective input of a running counter within the declared timeout interval, then the transmitter error flag (**indicate**) is changed to 1 and the corresponding error bit (**ERR**) is on, triggering a forced output switchoff and F-LED is on.

NOTE: In operating modes 6 and 7 count pulse monitoring is not supported. Refer to *Operating Modes*, page 53.

Monitoring Requirements

To activate signal monitoring, it is necessary to state a value between 1 and 255 in the parameter configuration screen for **Counter Watchdog Time**. This fixes the counter's watchdog timers within the limits from 100 ms to 25.5 s.

Counting pulse monitoring for the respective counter occurs when the counting pulse is enabled and the counter is running. The prerequisite is the specification of a watchdog time.

NOTE: No monitoring is performed for 0 values.

Overflow Notification

Overflow notification:

Mode	Description
Up counting	The counter overflow is detected at an actual value of $> 2^{\exp(31)} - 1$.
Down counting	The counter overflow is detected at an actual value of $> 2^{\exp(31)}$.

NOTE: For further information see *EHC 105 00 High Speed Counter Module Description*, page 71.

Quantum System Bus Monitoring

Monitoring Function

A "system active" signal is activated on the Quantum system bus. If the CPU fails, all outputs are set accordingly and the green ACTIVE status LED turns off.

Output Behavior

The status of the outputs in the event of a communication failure between the controller and the EHC 105 00 can be selected through the EBUA output register bit (4x...).

Signal	Meaning
1	The current output state is retained.
0	All employed outputs are set to 0 level.

US24 Monitoring

Monitoring Function

If...	Then ...
the external 24VDC power supply fails during operation,	<ul style="list-style-type: none">● the green P-LED turns off and is shown in the module status byte,● and the red F-LED turns on.
the power returns,	<ul style="list-style-type: none">● the P-LED turns on,● and the F-LED turns off.

Output Behavior

The discrete output (OUT1...OUT8) status displays (1 to 8) turn off; independent of the defined output logic (positive or negative).

An output switchoff is not triggered for a running counter.

Start-Up Characteristics

What Happens at Start-Up

At EHC 105 00 startup the following happens:

Stage	Description
1	All actual values are cleared to 0.
2	Outputs are deactivated (that is VA1E = VA2E = E/SE = 0).
3	The counters are defaulted to: <ul style="list-style-type: none"> • upevent counters, • absolute output set point values (VAR = 0) and • outputs in operating mode A (timed control mode).
4	Outputs are set to 0 (EBUA = 0) on controller communications failure with the EHC105.
5	By default, all counters are enabled.

Assignments for Discrete I/O

Start-up assignment for discrete I/O

Counter Input/Output	Discrete Signal	Pin Assignments
Counter 1		
LS1 (Load and Start)	IN1	21
ST1 (Restart)	IN1	21
BEA1 (Output switch-off)	IN6	26
Counting Pulse 1	5C1/24C1	1/11
VA2E1	OUT6	36
E/SE1	OUT1	31
Counter 2		
LS2 (Load and Start)	IN2	22
ST2 (Restart)	IN2	22
Counting Pulse 2	5C2/24C2	3/13
E/SE2	OUT2	32

Counter Input/Output	Discrete Signal	Pin Assignments
Counter 3		
LS3 (Load and Start)	IN3	23
ST3 (Restart)	IN3	23
BEA3	IN7	27
Counting Pulse 3	5C3/24C3	5/15
VA2E3	OUT7	37
E/SE3	OUT3	33
Counter 4		
LS4 (Load and Start)	IN4	24
ST4 (Restart)	IN4	24
Counting Pulse 4	5C4/24C4	7/17
E/SE4	OUT4	34
Counter 5		
LS5 (Load and Start)	IN5	25
ST5 (Restart)	IN5	25
Counting Pulse 5	5C5/24C5	9/19
BEA5	IN8	28
VA2E5	OUT8	38
E/SE5	OUT5	35

Part II

EHC 105 00 High Speed Counter Module Description

Chapter 6

EHC 105 00 High Speed Counter Module Description

Introduction

This chapter includes information about the module description for EHC 105.

What Is in This Chapter?

This chapter contains the following topics:

Topic	Page
Presentation	72
EHC 105 00 Hardware Configuration	74
Indicators	77
Wiring	78
Specifications	81
EHC 105 00 Hardware Specifics	83

Presentation

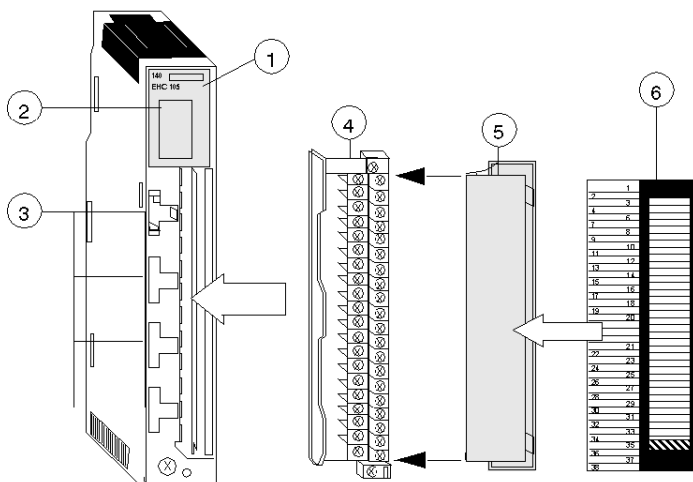
Function

The 140 EHC 105 00 is a highspeed counter module. It utilizes five equivalent, independently usable counters with the following functions:

- 32bit event counter with 6 modes
 - Event counter with parallel set point output activation
 - Event counter with parallel set point output activation and fast Final Set Point
 - Event counter with serial set point activation
 - Event counter with serial set point activation and fast final set point
 - Event counter with timed set point output activation
 - Event counter with latched set point output activation
- 32bit differential counter (2 configurable counter pairs) with 2 modes
 - Differential counter with serial set point output activation
 - Differential counter with parallel set point output activation
- 16bit repetitive counter
- 32bit (velocity counter, rate counter) with 2 modes
 - Rate counter with 100ms gate time
 - Rate counter with 1s gate time

Illustration

The following figure shows the EHC 105 module and its components.



- 1 Model Number, Module Description, Color Code
- 2 LED Display
- 3 Fuse Cutouts
- 4 Field Wiring Terminal Strip
- 5 Removable Door
- 6 Customer Identification Label (Fold label and place it inside door)

NOTE: The field wiring terminal strip (Modicon #140 XTS 002 00) must be ordered separately. (The terminal strip includes the removable door and label.)

EHC 105 00 Hardware Configuration

Voltage Supply

The EHC 105 00 module is supplied by the Quantum bus with VCC = 5 VDC. The isolated I/O and the counter inputs are an exception. They receive the working voltage US24 = 24 VDC provided by an external power supply. The green P-LED lights when US24 is present.

In addition, if the 24 VDC is not present, status bit 7 is set and the FLED turns on. If the 24 VDC is present again, status bit 7 is reset and the FLED turns off.

NOTE: The alternatively available 5 VDC counter inputs may also be used.

Hot Swap

As for all Quantum modules, you can remove and insert the module during bus operation. However, module reconfiguration is required.

Counter Inputs

The counter inputs are isolated from one another and from the discrete I/O. Each counter input is present in two variations, whereby 5C1...5C5 are for 5 VDC signals and 24C1...24C5 for 24 VDC signals.

All input signals are displayed by green LEDs. (Refer to *Indicators*, page 77).

WARNING

RISK OF HARDWARE CONFIGURATION FAILURE

Only connect transmitters with 5 VDC output signals to 5C1...5C5.

Only use one connection (either 5 VDC or 24 VDC) from each counter input.

Failure to follow these instructions can result in death, serious injury, or equipment damage.

Counter Input Example

There is exactly one reference potential per counter input (M11...M15):

- 5 VDC transmitter on counter 4: using terminals 5C4 and M14
- 24 VDC transmitter on counter 4: using terminals 24C4 and M14

Counter Enable

To every counter a hardware-related input (IN1...IN5) is assigned as counter enable (gate function). Whether the input is to be used as counter enable can be selected separately for each counter channel through the parameter configuration. The input may be used for other functions, should it not be allocated as counter enable. The counter input is then always enabled.

Discrete Inputs

The module is equipped with five counter and eight discrete inputs, each of which can be assigned different functions.

Discrete inputs are isolated from the back plane.

All input signals are displayed by green LEDs. (Refer to *Indicators*, [page 77](#)).

The discrete inputs can be assigned the following functions:

- Counter enable (gate function)
- Counter load/start (outputs set)
- Counter restart (outputs set)
- Output switchoff trigger (resets outputs VA1Ex, VA2Ex and E/SEx)
- Input signal states can be inverted

NOTE: Notice following:

- The load/start respectively restart functions are combined by a logical AND with the LSx respectively STx state RAM bits.
- If no hardware input is utilized for load/store respectively restart, then the AND condition is met, if the bit in state RAM is set.
- In the event counter modes (operating modes 1 and 2) and differential counter mode (operating modes 3 and 4), the restart command is only possible after an output switchoff (BEAx).
- The restart command is not possible in the repetitive counter (mode 5), velocity counter (modes 6 and 7), and event counter with fast output switchoff (modes 8 and 9) operating modes.

Discrete Outputs

The module has eight discrete outputs. All outputs are short circuit proof and overloadproof ($I_{max} = 500 \text{ mA}$), and have potential isolation with respect to the inputs and back plane (I/O bus).

To the outputs the following functions can be assigned:

- First set point (timed for mode A)
- Second set point (timed for mode A)
- Final set point (timed for mode A)
 - Module outputs assigned to the final set point of those operating modes making use of the fast final set point are processed particularly fast:
 - without fast final set point: typically 3 ms
 - with fast final set point: typically 0.5 ms
- Timed final set point (with choice of pulse width)
- Output signal states can be inverted

Short Circuit

Short circuit of one or more outputs leads to a fault message (the red F-LED lights). As soon as the short circuit has been neutralized, the outputs can be returned to normal operation per collective reset signal Q.

Power-Up

At powerup (back plane 5 VDC) all discrete outputs are inactive. On master station failure all outputs are deactivated. (The outputs go to 0 with positive logic and 1 with negative logic).

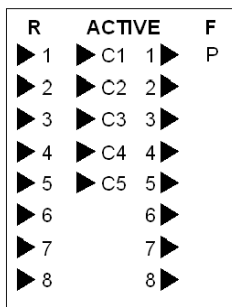
Jumpers

The module is delivered without jumpers. The module's contact strips are only used for test purposes.

Indicators

Illustration

The following table shows the LED indicators for the EHC 105 module.



Description

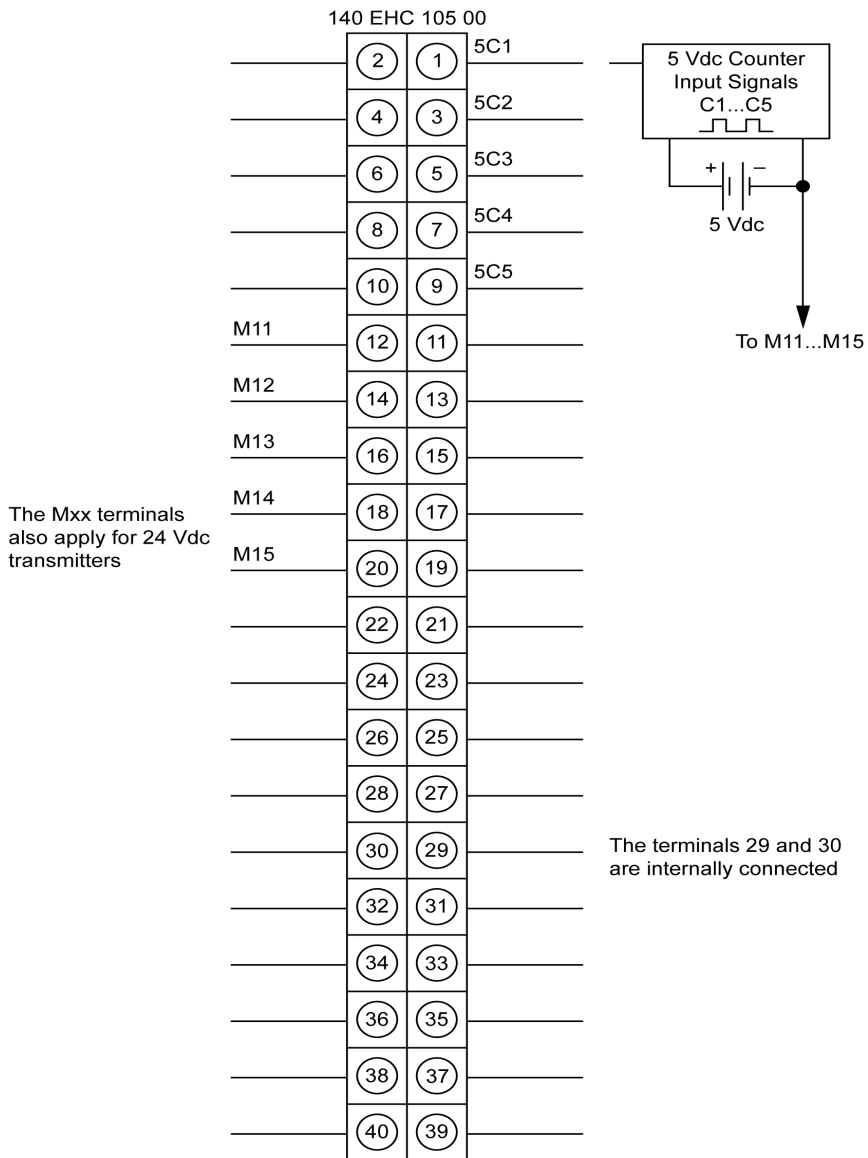
The following table shows the LED descriptions for the EHC 105 module

LED	Color	Description
R	green	Module is READY (firmware initialization has been completed).
P	green	POWER - the US24 working voltage is present.
F	red	The red F-LED (F = fault) lights on the following faults: <ul style="list-style-type: none"> ● 24 VDC supply voltage (US24) not present ● Short circuit on one of the OUTn outputs ● Pulse monitoring has tripped (indicate bit = 1 and ERRx = 1) ● Counter overflow (indicate bit = 0 and ERRx = 1)
ACTIVE	green	The PLC communication becomes active.
1 to 8	green	Displays the signal states of the discrete inputs IN1...IN8.
1 to 8	green	Displays the signal states of the discrete outputs OUT1...OUT8.
C1 to C5	green	Lights with the clock frequency applied to clock-inputs 5C1 to 5C5 respectively 24C1 to 24C5.

Wiring

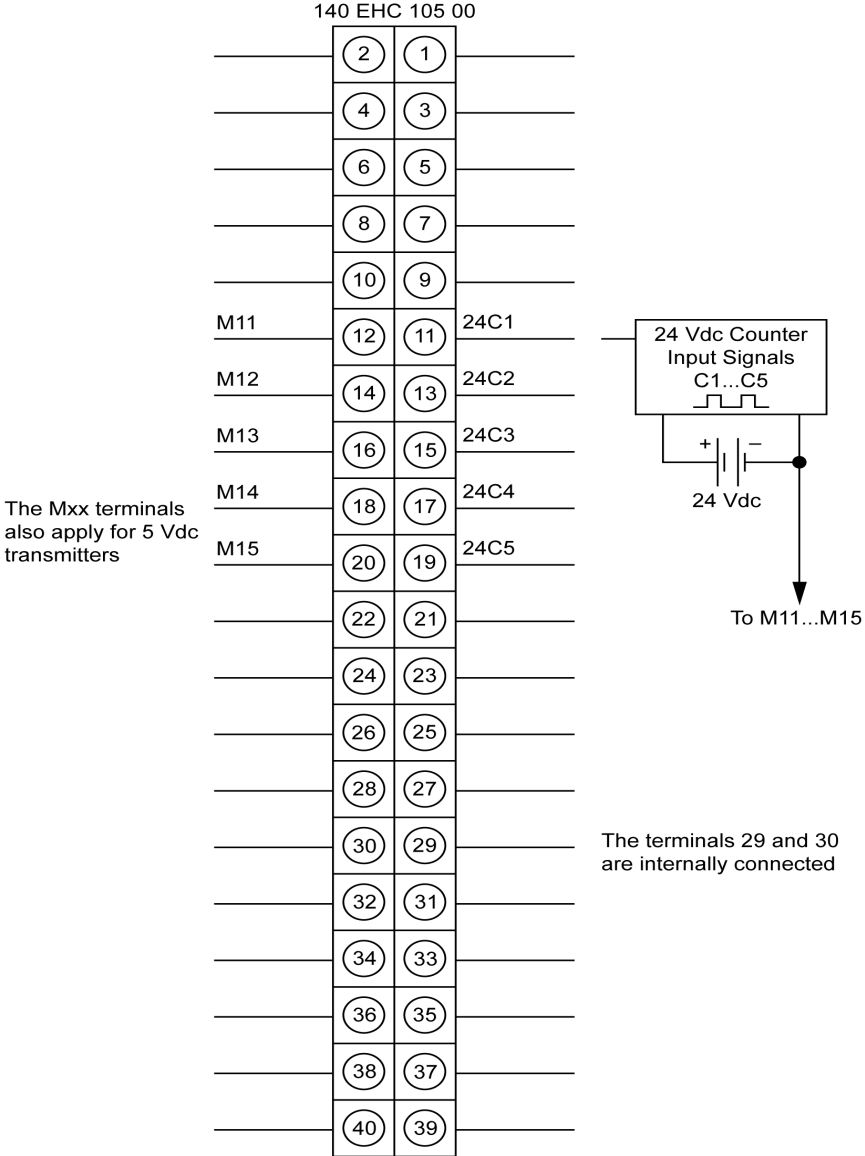
5Cx Counter Inputs

Wiring diagram for 5Cx counter inputs:



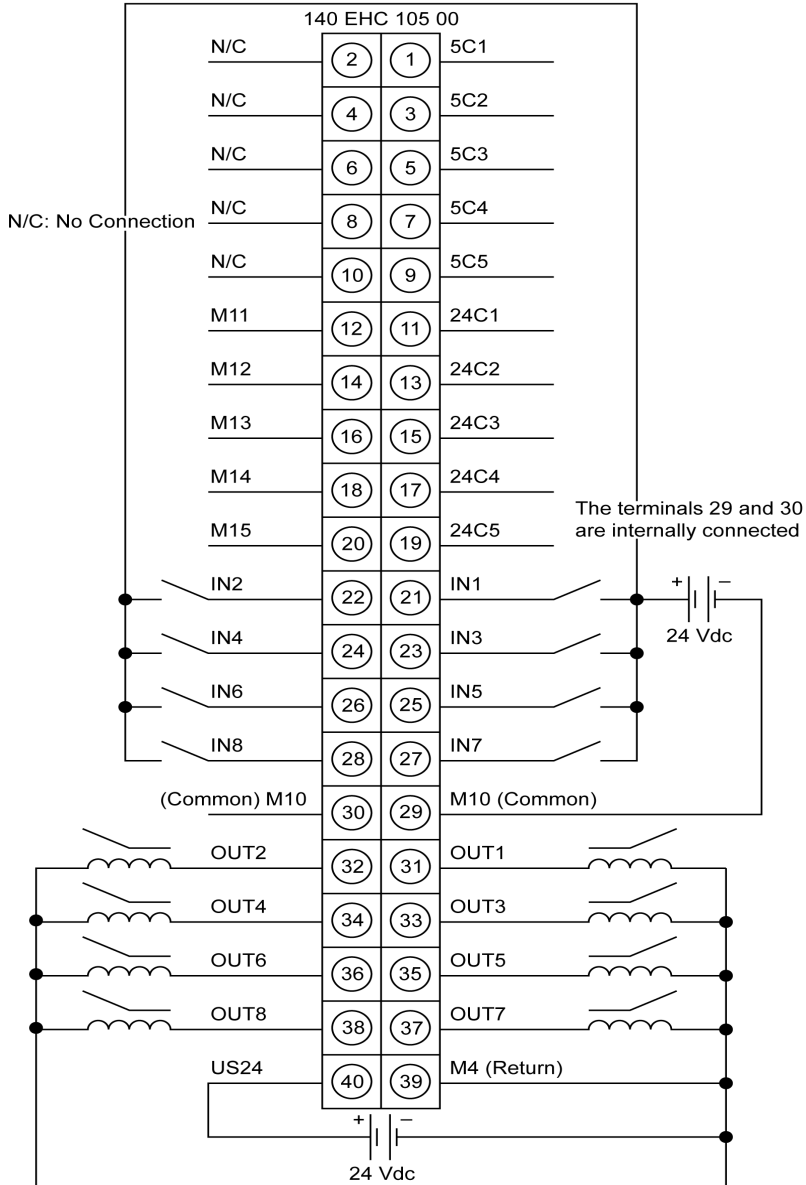
24Cx Counter Inputs

Wiring diagram for 24Cx counter inputs:



Discrete Inputs and Outputs

Wiring diagram for discrete inputs and outputs:



Specifications

General Specifications

General Specifications

Module Type	High Speed Counter Module
Number of Channels	5
External Power	19,2 ... 30 VDC, 24 VDC nominal, 60 mA required plus the load current for each output.
Power Dissipation	Maximum 6W
Bus Current required	250 mA
I/O Map	12 words IN, 13 words OUT
Isolation (channel to bus)	500 VAC rms for 1 minute
Fault detection	Loss of output field power, output short circuit
Fusing	internal: none external: user discretion
Backplane Support	Local, remote or distributed
Compatibility	All Quantum Controllers, V2.0 at a minimum

NOTE: The 5Cx and 24Cx counter inputs may be used alternatively.

Counter Inputs

Counter Inputs

Counter Inputs	5V	24V
Count frequency	100 kHz	20 kHz
Count to output assertion delay (Max)	3ms	
Input voltage	OFF state (VDC) :1,0 ... +1,15 ON state (VDC): 3,1 ... 5,5	OFF state (VDC): -3,0 ... +5,0 ON state (VDC):15,0 ... 30,0
Input current	8 mA for 3,1VDC	7 mA for 24 VDC
Duty cycle	1 : 1	
Data formats	16 bit counter: 65.535 Decimal 32 bit counter: 2.147.483.647 Decimal	
Delay time (typical)	t = 0,002 ms	
Operating mode	discrete incremental counter	

Discrete Inputs

Discrete Inputs

Discrete Inputs	24V
VREF supply +24VDC	Off State (VDC): -3,0 ... +5,0 ON State (VDC):15,0 ... 30,0
Delay time (typical) IN1 ... IN6 IN7, IN8	ton = 2,2 ms, toff = 1 ms ton = 0,006 ms, toff = 0,3 ms
Input current (typical)	5 mA

Input Threshold

Input Threshold

single ended mode	5 VREF DC	-
	12 VREF DC	-
	24 VREF DC	-3 ... 5 V on state/15 ... 30 off state
differential mode		-

Discrete Outputs

Discrete Outputs

Output Voltage	24V
FET Switch ON	20 ... 30 VDC
FET Switch OFF	0 VDC (ground reference)
Max load current (each output)	0,5 A
Output off state Leakage	0,1 mA max @ 30 VDC
Output on state voltage drop	1,5 VDC @ 0,5 A

EHC 105 00 Hardware Specifics


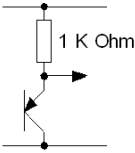
Cable Specifics

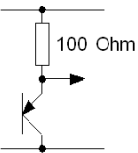
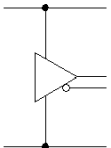
The cable specifics are as follows:

- Shielded, twisted pair cable is to be utilized for pulse generator connection to the counter inputs.
 - JELiYCY 2 X 2 X 0.5 (Order no.: 424 234 035)
 - JELiYCY 5 X 2 X 0.5 (Order no.: 424 238 059)
- The shield should have a short connection (< 20 cm) with ground at one cable end.
- Be sure not to install the cabling together with power lines or other similar sources of electrical disturbance. Clearance > 0.5 m.
- Input connecting cables, bulk:
 - JELiYCY 2 X 2 X 0.5 twisted pair, (Order no.: 424 234 035).
 - JELiYCY 5 X 2 X 0.5 twisted pair, (Order no.: 424 238 059).

NOTE: Pay attention to cable length dependencies upon transmitter frequencies and output type.

Maximum Cut-Off Frequencies

Transmitter Output	Circuit Diagram	Transmitter Output Level(VDC)	Cable Length (m)	Max. Transmitter Frequency (KHz)
Push-Pull Driver	Push-pull (24) 	24 24 24	30 100 300	35 20 10
NPN Driver (open collector)	NPN (24) 	24 24 24	30 100 300	35 20 10

Transmitter Output	Circuit Diagram	Transmitter Output Level(VDC)	Cable Length (m)	Max. Transmitter Frequency (KHz)
NPN Driver (open collector)	NPN (5) 	5 5	30 300	100 100
SN 75 178 line driver	SN 75 178 (5) 	5 5	30 300	100 100

Part III

EHC 105 00 Configuration

Purpose

This part provides information on the configuration of the 140 EHC 105 00 High Speed counter module.

What Is in This Part?

This part contains the following chapters:

Chapter	Chapter Name	Page
7	Quantum Addressing Modes	87
8	Registers and Datatypes	93
9	Software Configuration	113
10	Configuration Examples	121

Chapter 7

Quantum Addressing Modes

Purpose

This chapter provides information on the three different modes Control Expert allows to address the I/O data from a Quantum I/O module:

- Flat Addressing
- Topological Addressing
- IODDT Addressing

NOTE: Topological addresses overlapping (%IW_r.m.c) is not supported by Quantum application, use flat addressing (%IW_x) when memory overlapping control is needed.

NOTE: The different addressing modes refer to the same physical location in the PLC memory for a given data point.

While Flat Addressing and Topological Addressing are available for all Quantum I/O modules, IODDTs are only provided for modules that deliver information in addition to the I/O values (e.g. errors or warnings).

Also provided is information about I/O module status bytes and bit order.

What Is in This Chapter?

This chapter contains the following topics:

Topic	Page
Flat Addressing—800 Series I/O Modules	88
Topological Addressing—800 Series I/O Modules with Control Expert	89
IODDT Addressing	90
Addressing Example	91
Discrete I/O Bit Numbering	92

Flat Addressing—800 Series I/O Modules

Introduction

800 series I/O modules follow a system of flat address mapping in Control Expert. To work properly, each module requires a determinate number of bits and/or words. The IEC addressing system is equivalent to the 984LL register addressing. Use the following assignments:

- 0x is now %Mx
- 1x is now %Ix
- 3x is now %IWx
- 4x is now %MWx

The following table shows the relationship between 984LL notation and IEC notation.

Outputs and Inputs	984LL Notation Register Addresses	IEC Notation		
		System Bits and Words	Memory Addresses	I/O Addresses
output	0x	System Bit	%Mx	%Qx
input	1x	System Bit	%Ix	%Ix
input	3x	System Word	%IWx	%IWx
output	4x	System Word	%MWx	%QWx

To access the I/O data of a module,

Step	Action
1	Enter the address range in the configuration screen.

Examples

The following examples show the relationship between 984LL register addressing and IEC addressing:

000001 is now %M1

100101 is now %I101

301024 is now %IW1024

400010 is now %MW10

Topological Addressing—800 Series I/O Modules with Control Expert

Accessing I/O Data Values

Use topological addressing to access I/O data items. Identify the topological location of the module within an 800 series I/O module with Control Expert using the following notation:

```
%<Exchangetype><Objecttype>[\b.e\]r.m.c[.rank]
```

where:

- **b** = bus
- **e** = equipment (drop)
- **r** = rack
- **m** = module slot
- **c** = channel

NOTE: When addressing,

1. The [b.e] defaults to \1.1\ in a local rack and does not need to be specified.
2. The rank is an index used to identify different properties of an object with the same data type (value, warning level, error level).
3. The rank numbering is zero-based, and if the rank is zero, omit the entry.

For detailed information on I/O variables, please refer to the *EcoStruxure™ Control Expert, Program Languages and Structure, Reference Manual*.

Reading Values: An Example

To read	Action
input value (rank = 0) from channel 7 of an analog module located in slot 6 of a local rack:	Enter %IW1.6.7[.0]
input value (rank = 0) from channel 7 of an analog module located in slot 6 of drop 3 of RIO bus 2:	Enter %IW\2.3\1.6.7[.0]
'out of range' value (rank = 1) from channel 7 of an analog module located in slot 6 of a local rack:	Enter %I1.6.7.1[.0]

IODDT Addressing

IODDT Addressing

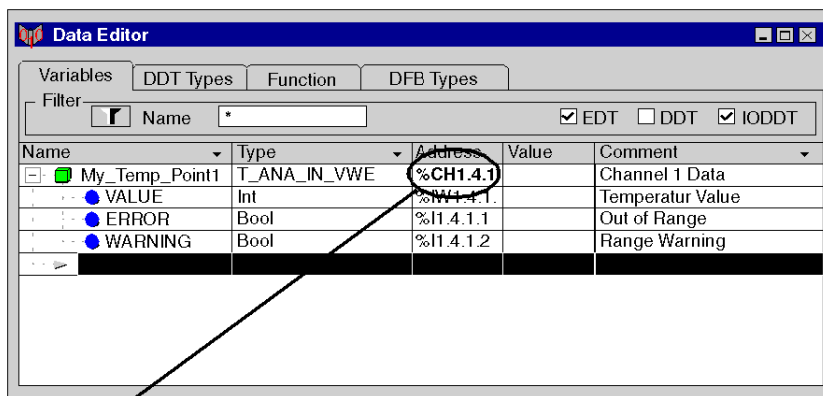
An IODDT allows all information (bits and registers) related to a channel to be handled through a user-defined variable. This variable is defined in the Control Expert data editor by selecting the appropriate IODDT for the module as a data type and specifying the topological address of the module using the following syntax:

```
%CH[\b.e\]r.m.c
```

where:

- **b** = bus
- **e** = equipment (drop)
- **r** = rack
- **m** = module slot
- **c** = channel

Here is an example of an IODDT for a thermocouple input module in slot 4 of a local rack:



Note: Only %CH1.4.1 needs to be entered. The topological addresses related to this channel (%IW.. and %I..) are generated automatically.

Variables in the User Program

You can access all information related to channel 1 of the module using the following variables:

- My_Temp_Point1.VALUE for the measured value
- My_Temp_Point1.ERROR indicating an out-of-range condition
- My_Temp_Point1.WARNING indicating an over-range condition

Addressing Example

Comparing the 3 Addressing Modes

The following example compares the 3 possible addressing modes. An 8-channel thermocouple 140 ATI 030 00 module with the following configuration data is used:

- mounted in slot 5 of the CPU rack (local rack)
- starting input address is 201 (input word %IW201)
- end input address is 210 (input word %IW210)

To access the I/O data from the module you can use the following syntax:

Module data	Flat Addressing	Topological Addressing	IODDT Addressing	Concept Addressing
Channel 3 temperature	%IW203	%IW1.5.3	My_Temp.VALUE	300203
Channel 3 out of range	%IW209.5	%I1.5.3.1	My_Temp.ERROR	300209 Bit 5 to be extracted by user logic
Channel 3 range warning	%IW209.13	%I1.5.3.2	My_Temp.WARNING	300209 Bit 13 to be extracted by user logic
Module internal temperature	%IW210	%IW1.5.10	not accessible through IODDT	300210

NOTE: For the IODDT the data type `T_ANA_IN_VWE` is used and the variable `My_Temp` with the address `%CH1.5.10` was defined.

For comparison, the register addressing as used with Concept is added in the last column. As Concept does not support direct addressing of a bit in a word, the bit extraction has to be performed in the user program.

Discrete I/O Bit Numbering

Introduction

The numbering of channels of an I/O module usually starts with 1 and counts up to the maximum number of supported channels. The software however starts numbering with a 0 for the least significant bit in a word (LSB). The Quantum I/O modules have their lowest channel mapped to the most significant bit (MSB).

The following figure shows the mapping of I/O channels related to the bits in a word:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	I/O Channels															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit numbering															
MSB																LSB															

Word Addressing Versus Bit Addressing

Mainly discrete I/O modules can be configured to deliver their I/O data either in word format or in bit format. This can be selected during configuration by selecting either `%IW` (`%MW`) or `%I` (`%M`). If you need to access a single bit from an I/O module configured to use an I/O word, you can use the syntax `%word.bit`. The following table gives you the connection between I/O point number and the associated I/O address in bit and word addressing.

The table shows a 32-point input module in the main rack, slot 4 configured with starting address `%I1` or `%IW1`:

I/O channel	Bit address (flat addressing)	Bit address (topological addressing)	Bit address extracted from word (flat addressing)	Bit address extracted from word (topological addressing)
1	<code>%I1</code>	<code>%I1.4.1[.0]</code>	<code>%IW1.15</code>	<code>%IW1.4.1.1.15</code>
2	<code>%I2</code>	<code>%I1.4.2[.0]</code>	<code>%IW1.14</code>	<code>%IW1.4.1.1.14</code>
3	<code>%I3</code>	<code>%I1.4.3[.0]</code>	<code>%IW1.13</code>	<code>%IW1.4.1.1.13</code>
...				
15	<code>%I15</code>	<code>%I1.4.15[.0]</code>	<code>%IW1.1</code>	<code>%IW1.4.1.1.1</code>
16	<code>%I16</code>	<code>%I1.4.16[.0]</code>	<code>%IW1.0</code>	<code>%IW1.4.1.1.0</code>
17	<code>%I17</code>	<code>%I1.4.17[.0]</code>	<code>%IW2.15</code>	<code>%IW1.4.1.2.15</code>
18	<code>%I18</code>	<code>%I1.4.18[.0]</code>	<code>%IW2.14</code>	<code>%IW1.4.1.2.14</code>
...				
31	<code>%I31</code>	<code>%I1.4.31[.0]</code>	<code>%IW2.1</code>	<code>%IW1.4.1.2.1</code>
32	<code>%I32</code>	<code>%I1.4.32[.0]</code>	<code>%IW2.0</code>	<code>%IW1.4.1.2.0</code>

Chapter 8

Registers and Datatypes

Purpose

This chapter provides information on registers and datatypes of the 140 EHC 105 00 High Speed counter module.

What Is in This Chapter?

This chapter contains the following sections:

Section	Topic	Page
8.1	Communication	94
8.2	State RAM structure (3x)	95
8.3	State RAM structure (4x)	100
8.4	Derived Data Types (IODDT)	107
8.5	Topological Addressing	110

Section 8.1

Communication

State RAM Communication

Overview

The following description of the communication between the 140 EHC 105 and the CPU is based on the register addressing established in the Quantum world. For Control Expert this addressing is replaced by the three addressing modes described in *Flat Addressing—800 Series I/O Modules*, [page 88](#), *Topological Addressing—800 Series I/O Modules with Control Expert*, [page 89](#) and *IODDT Addressing*, [page 90](#).

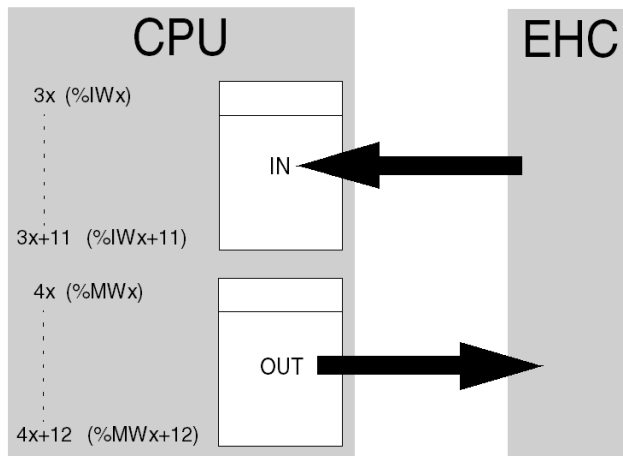
To correctly interpret the address information given in the following sections you can replace all **3x** references by **%IWx** and all **4x** references by **%MWx**.

To make use of the advanced addressing features of Control Expert please refer to *Topological Addressing*, [page 110](#) and *Derived Data Types (IODDT)*, [page 107](#).

The communication is managed by the following registers in the State RAM:

- **3x-Register (%IWx)**: to transfer status information and counting values from the EHC to the CPU
- **4x-Register (%MWx)**: to transfer the parameters of the I/O configuration from the CPU to the EHC

This diagram shows the communication between the EHC 105 00 and the CPU.



Section 8.2

State RAM structure (3x)

Purpose

This section provides information on the state RAM structure (3x) of the 140 EHC 105 00.

What Is in This Section?

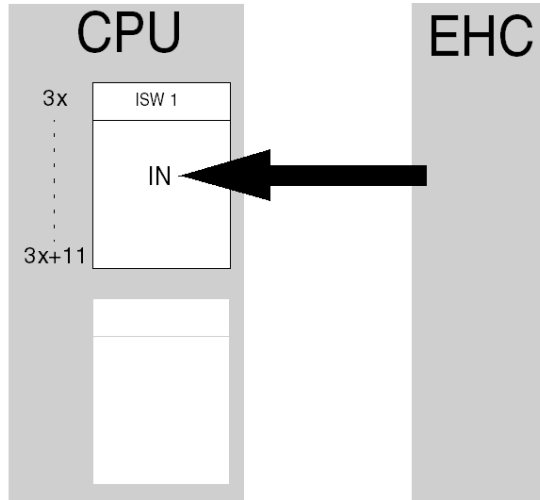
This section contains the following topics:

Topic	Page
Input Structure	96
Input Status Words	98

Input Structure

Overview

This diagram shows the input structure of the communication between the EHC 105 00 and the CPU.



3x-Register assignment

This table shows the 3x-Register assignment of the EHC 105.

Register		Assignment
3x		Input status word 1 (ISW 1)
3x+1		Input status word 2 (ISW 2)
3x+2	Low word	Counter 1: actual value
3x+3	High word	
3x+4	Low word	Counter 2: actual value
3x+5	High word	
3x+6	Low word	Counter 3: actual value
3x+7	High word	
3x+8	Low word	Counter 4: actual value
3x+9	High word	
3x+10	Low word	Counter 5: actual value
3x+11	High word	

Input Status Words

Purpose

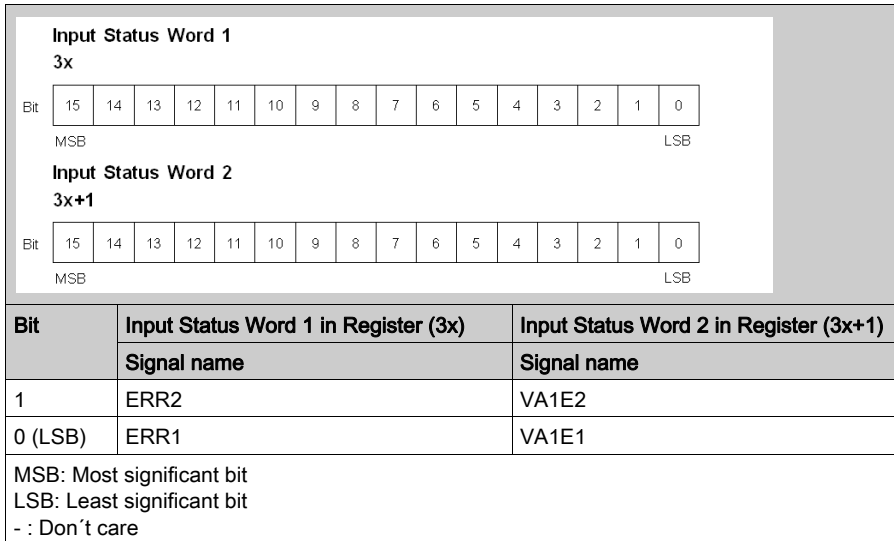
There are two input status words, stored in successive 3x-Registers in the State RAM of the controller.

They carry diagnostic information about the status of the EHC 105 00

Input Status Words

This table shows the assignment of every bit in the input status words

Input Status Word 1 3x																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB															LSB
Input Status Word 2 3x+1																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB															LSB
Bit	Input Status Word 1 in Register (3x)								Input Status Word 2 in Register (3x+1)							
	Signal name								Signal name							
15 (MSB)	--								--							
14	--								--							
13	--								--							
12	E/SE5								VA2E5							
11	E/SE4								VA2E4							
10	E/SE3								VA2E3							
9	E/SE2								VA2E2							
8	E/SE1								VA2E1							
7	US24								--							
6	SC								--							
5	INDICATE								--							
4	ERR5								VA1E5							
3	ERR4								VA1E4							
2	ERR3								VA1E3							



Parameters

This table shows the parameters of the input status word 1

Parameter	Value (Hex)	Meaning
ERRx	1	Error in counter (see INDICATE)
INDICATE	0	Counter overflow (i.e. actual value > (2 exp 31)-1)
	1	Counting pulse error (counter timeout value expired)
SC	1	Discrete output short circuit or overload
US24	1	External power failure
E/SEx	1	Final set point signal on counter x = "1"

This table shows the parameters of the input status word 2

Parameter	Value (Hex)	Meaning
VA1Ex	1	First set point signal on counter x = "1"
VA2Ex	1	Second set point signal on counter x = "1"

Section 8.3

State RAM structure (4x)

Purpose

This section provides information on the State RAM structure (4x) of the 140 EHC 105 00.

What Is in This Section?

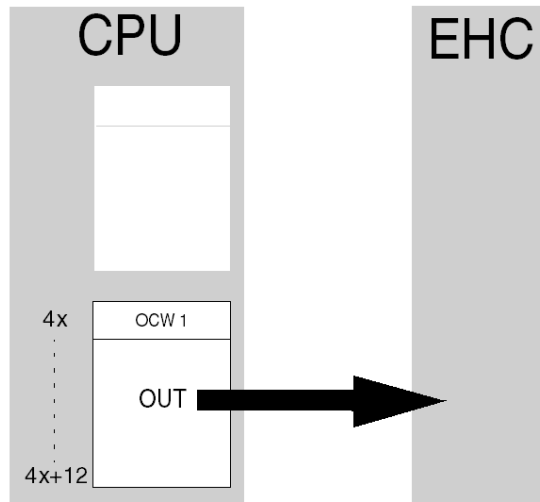
This section contains the following topics:

Topic	Page
Output Structure	101
Output Control Words (OCW)	103

Output Structure

Overview

This diagram shows the output structure of the communication between the EHC 105 00 and the CPU.



4x-Register assignment

This table shows the 4x-Register assignment of the EHC 105.

Register		Assignment	
4x		<i>Output Control Words (OCW), page 103</i>	OCW 1
4x+1			OCW 2
4x+2			OCW 3
4x+3	Low word	Counter 1	Stop value for VR1="0", Final set point value E/S1
4x+4	High word		Initial value for VR1="0", Final set point value E/S1
4x+5	Low word	Counter 2	Stop value for VR2="0", Final set point value E/S2
4x+6	High word		Initial value for VR2="0", Final set point value E/S2
4x+7	Low word	Counter 3	Stop value for VR3="0", Final set point value E/S3
4x+8	Low word		Initial value for VR3="0", Final set point value E/S3
4x+9	Low word	Counter 4	Stop value for VR4="0", Final set point value E/S4
4x+10	Low word		Initial value for VR4="0", Final set point value E/S4
4x+11	Low word	Counter 5	Stop value for VR5="0", Final set point value E/S5
4x+12	Low word		Initial value for VR5="0", Final set point value E/S5

NOTE: The 4x-Register assignment along with the *OCW Parameter Settings, page 105* is used for the *I/O Configuration, page 114* of the module

Output Control Words (OCW)

Purpose

There are three output control words, stored in successive 4x-Registers in the State RAM of the controller.

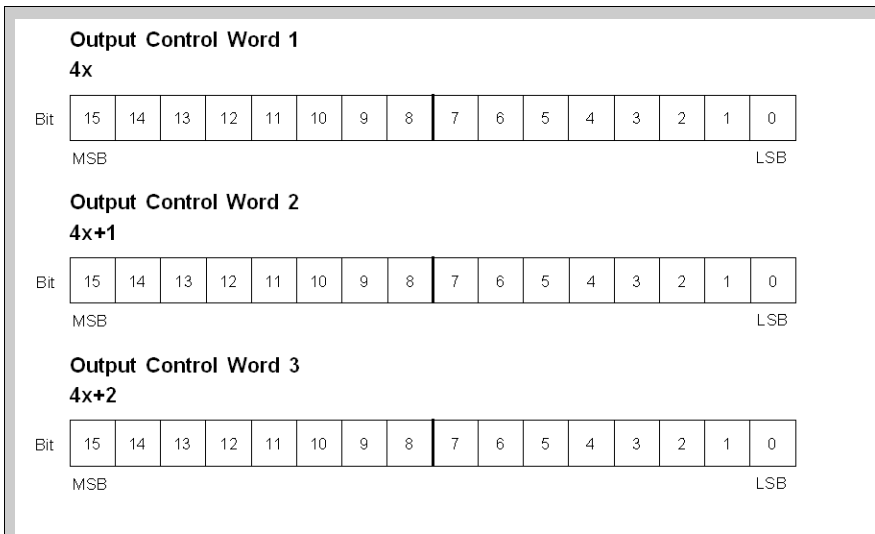
They contain parameters, which can be set

- for **each** counter separately:
 - operating mode
 - counting direction etc.
- for **all** counters in general:
 - output behaviour
 - error acknowledgement etc.

Output Control Words

This table shows the assignment of every bit in the Output Control Words

Output Control Word 1 4x																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB								LSB							
Output Control Word 2 4x+1																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB								LSB							
Output Control Word 3 4x+2																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSB								LSB							
Bit	Output control word 1 in Register 4x		Output control word 2 in Register 4x+1		Output control word 3 in Register 4x+2											
	Signal name		Signal name		Signal name											
15 (MSB)	Counter 1 operating mode		Counter 3 operating mode		Counter 5 operating mode											
14	See following table		See following table		See following table											
13																
12																



Bit	Output control word 1 in Register 4x	Output control word 2 in Register 4x+1	Output control word 3 in Register 4x+2
	Signal name	Signal name	Signal name
11	VR1	VR3	VR5
10	BEA1	BEA3	BEA5
9	ST1	ST3	ST5
8	LS1	LS3	LS5
7	-	Counter 2 operating mode See following table	Counter 4 operating mode See following table
6	-		
5	EBUA		
4	VAR		
3	-	VR2	VR4
2	-	BEA2	BEA4
1	FQ	ST2	ST4
0 (LSB)	Q	LS2	LS4
MSB: Most significant bit LSB: Least significant bit - : Don't care			

OCW Parameter Settings

This table shows the setting of OCW parameters referring to each counter

Parameter	Value (Hex)	Meaning
Counter x Operating mode	1	Event counter with parallel Set Point activations
	2	Event counter with serial Set Point activations
	3	Differential counter with parallel Set Point activations only applies to counter 1 and counter 3
	4	Differential counter with serial Set Point activations only applies to counter 1 and counter 3
	5	Repetitive counter
	6	Rate counter, gate time $t = 100$ ms
	7	Rate counter, gate time $t = 1$ s
	8	Event counter with parallel Set Point activations and fast final Set point
	9	Event counter with serial Set Point activations and fast final Set point
	A (Default)	Event counter with timed "on" outputs, the pulse width setting holds for all employed outputs
	B	Event counter with latched Set points outputs
	0, C, D, E, F	Event counter with timed "on" outputs, the pulse width setting holds for all employed outputs (identical with "A")
VRx	0	Counter x counts up
	1	Counter x counts down
BEAx	1	Counter x Output Switch-off
STx	1	Counter x restart (controlled by rising edge)
LSx	1	Counter x load/start (controlled by rising edge)

This table shows the setting of general OCW parameters referring to all counters

Parameter	Value (Hex)	Meaning
EBUA	0	Outputs turn to "0" on communication errors
	1	Outputs retain their current states on communication errors
VAR	0	Values for Output Set points are absolute for all counters
	1	Values for Output Set points are relative for all counters
Q	1	Acknowledgement for all counter channels after an output short circuit fault signal (SC) Result: The red LED (F) extinguishes
FQ	4	Acknowledgement after counter errors (ERR1,...ERR5) Result: The red LED (F) extinguishes Note: Every error must be acknowledged individually Counter overflow can only be acknowledged after LS was active

Section 8.4

Derived Data Types (IODDT)

Purpose

This section provides information on the derived data types (IODDT) of the 140 EHC 105 00.

What Is in This Section?

This section contains the following topics:

Topic	Page
IODDT	108
T_CNT_EHC105_MOD	109

IODDT

Overview

This map presents a description of the T_CNT_105 IODDT of this module. An IODDT allows all information (bits and registers) related to a channel, to be handled through a user defined variable. For information about the usage of IODDTs please refer to *IODDT Addressing, page 90*.

NOTE: Deviating from this general description of the data types, in Quantum IODDTs for analog modules and expert modules the data type **Bool** is used for **%I** and **%Q**.

T_CNT_105

T_CNT_105 is used with all channels of the following I/O modules:

- EHC 105

The following IODDT for high speed counter module EHC 105 is valid for each of the 5 channels of the module.

Object	Symbol	Rank	Description
%IW	VALUE_L	1	Input value: Low word
%IW	VALUE_H	2	Input value: High word
%I	ERROR	1	Error in Counter
%I	SP_FINAL	2	Final Set Point signal
%I	SP_FIRST	3	First Set Point signal
%I	SP_SECOND	4	Second Set Point signal
%QW	STOP_VALUE	1	For CNT_DIR="0", final set point value
%QW	INITIAL_VALUE	2	For CNT_DIR="1", initial set point value
%Q	LS	1	"1", Counter load/start (controlled by the rising edge)
%Q	RSTART	2	"1", Counter restart (controlled by the rising edge)
%Q	OUT_OFF	3	"1", Counter output switch-off
%Q	CNT_DIR	4	"0" Counter counts up "1" Counter counts down
%Q	OM1	5	Operating Mode bit 1
%Q	OM2	6	Operating Mode bit 2
%Q	OM3	7	Operating Mode bit 3
%Q	OM4	8	Operating Mode bit 4

T_CNT_EHC105_MOD

Overview

This map presents a description of the T_CNT_EHC105_MOD IODDT of this module. The goal of this IODDT is to allow the user to handle all the information (bits and registers) that is related with the module.

Description

IODDT Description

Object	Symbol	Bit	Comment
%I.r.m.1.6	INDICATE	0	Counter overflow
		1	Counting pulse error
%I.r.m.1.7	SC	1	Discrete output short circuit
%I.r.m.1.8	US24	1	External power failure
%Q.r.m.1.1	Q	1	Acknowledgment after a short circuit failure
%Q.r.m.1.2	FQ	1	Acknowledgment after a counter error
%Q.r.m.1.5	VAR	0	Output set points are absolute for all counters
		1	Output set points are relative for all counters
%Q.r.m.1.6	EBUA	0	Outputs go to zero on communication errors
		1	Outputs retain their current state on communication errors

Section 8.5

Topological Addressing

Topological Addressing

Topological Addressing

The topological addressing allows to access I/O data items using the topological location of the module within a system.

Channel 1

Topological addresses for the data items of the first channel:

Symbol	Object	Description
VALUE_L	%IW[b.e]r.m.1.1	Input value: Low word
VALUE_H	%IW[b.e]r.m.1.2	Input value: High word
ERROR	%I[b.e]r.m.1.1	Error in Counter
SP_FINAL	%I[b.e]r.m.1.2	Final Set Point signal
SP_FIRST	%I[b.e]r.m.1.3	First Set Point signal
SP_SECOND	%I[b.e]r.m.1.4	Second Set Point signal
STOP_VALUE	%QW[b.e]r.m.1.1	For CNT_DIR="0", final set point value
INITIAL_VALUE	%QW[b.e]r.m.1.2	For CNT_DIR="1", final set point value
LS	%Q[b.e]r.m.1.1	"1", Counter load/start (controlled by the rising edge)
RSTART	%Q[b.e]r.m.1.2	"1", Counter restart (controlled by the rising edge)
OUT_OFF	%Q[b.e]r.m.1.3	"1", Counter output switch-off
CNT_DIR	%Q[b.e]r.m.1.4	"0" Counter counts up "1" Counter counts down
OM1	%Q[b.e]r.m.1.5	Operating Mode bit 1
OM2	%Q[b.e]r.m.1.6	Operating Mode bit 2
OM3	%Q[b.e]r.m.1.7	Operating Mode bit 3
OM4	%Q[b.e]r.m.1.8	Operating Mode bit 4

Used abbreviations: **b** = bus, **e** = equipment (drop), **r** = rack, **m** = module slot.

Channel 2 ... 5

The data for the channels 2 ... 5 can be accessed in the same way as channel 1 by setting the channel index according to the channel to be accessed:

%<Exchangetype><Objecttype>[\b.e]r.m.**channel.rank**

With channel = 1 ... 5.

General Parameters

The general module data can be accessed with channel index 6.

Topological addresses for the general parameters items of the module:

Symbol	Object	Description
INDICATE	%I[\b.e]r.m.6.1	"0" counter overflow "1" counter pulse error
SC	%I[\b.e]r.m.6.2	Discrete output short circuit or overload
US24	%I[\b.e]r.m.6.3	External power failure
Q	%Q[\b.e]r.m.6.1	Acknowledgment for all counter after an output short circuit
FQ	%Q[\b.e]r.m.6.2	Acknowledgment after counter errors
VAR	%QW[\b.e]r.m.6.3	"1" Output set points are relative for all the counters. "0" Output set points are absolute for all the counters.
EBUA	%QW[\b.e]r.m.6.4	"1" Output retain their current state on communications errors. "0" Outputs go to 0 signal in communication error.

Chapter 9

Software Configuration

Purpose

This chapter provides information on the software configuration of the 140 EHC 105 00 high speed counter module.

What Is in This Chapter?

This chapter contains the following topics:

Topic	Page
Software Configuration Process	114
Mapping a Local Quantum I/O Station	115
Access to Parameter Configuration	116
Parameter Configuration	117

Software Configuration Process

Overview

The software configuration of the 140 EHC 105 00 is divided in the following two parts:

- I/O Configuration and
- Parameter Configuration

For both parts of software configuration you find detailed examples in the chapter *Configuration Examples*, [page 121](#)

I/O Configuration

The I/O configuration includes:

- Setting the Final Set Point value for the eligible counter according to the *4x-Register assignment*, [page 102](#).
- Specifiing for each counter the characteristics (operating mode and counting direction) according to *OCW Parameter Settings*, [page 105](#)
- Specifiing the module characteristics (output behaviour and error acknowledgement) according to *OCW Parameter Settings*, [page 105](#)

Parameter Configuration

The *Parameter Configuration*, [page 117](#) includes:

- Addressing (i.e.mapping and range) and task of the module.
- Output and input behaviour for each counter

NOTE: You access the Parameter Configuration Screen with the Control Expert dialog: *Access to Parameter Configuration*, [page 116](#).

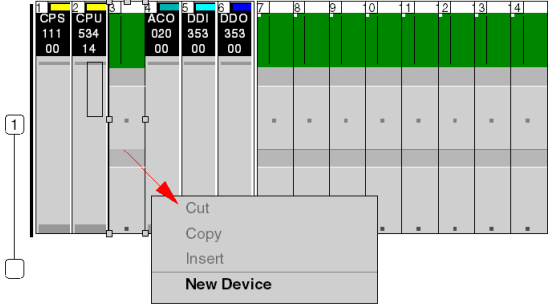
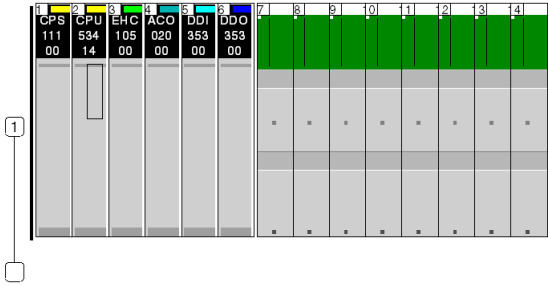
Mapping a Local Quantum I/O Station

Overview

Use the following dialog to map an existing local Quantum I/O station with the EHC 105.

Inserting a module (local)

This table provides the steps required for inserting a module in a local station.

Step	Action
1	Call the Bus Editor
2	Mark a free slot on the local station (left mouse button)
3	Move the mouse pointer over the marked slot
4	Click the right mouse button Result: A shortcut menu is opened
	
5	Select New device Result: A dialog window opens that displays all available modules
6	Select the EHC 105 module from the hardware catalog (from the counter category). Result: The new module is inserted in the empty slot on the local station.
	

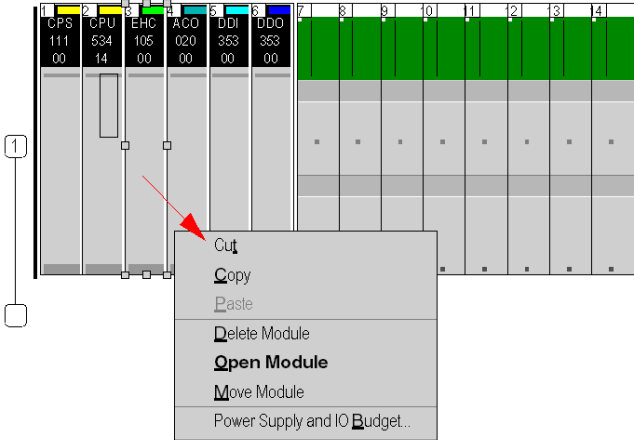
Access to Parameter Configuration

Overview

The following Control Expert dialog is necessary to access the module in preparation to the *Parameter Configuration*, page 117

Dialog to access the Parameter Configuration

This table shows the Control Expert dialog to access the Parameter Configuration

Step	Action														
1	Open the Bus Editor of Control Expert														
2	Select the EHC 105 00 module														
3	Click on the right mouse button Result: The context menu appears														
	 <p>The screenshot shows a grid of modules in the Bus Editor. The modules are labeled as follows:</p> <table border="1"> <thead> <tr> <th>Module</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>CPS</td> <td>111</td> </tr> <tr> <td>CPU</td> <td>534</td> </tr> <tr> <td>EHC</td> <td>105</td> </tr> <tr> <td>ACO</td> <td>020</td> </tr> <tr> <td>DDI</td> <td>353</td> </tr> <tr> <td>DDO</td> <td>353</td> </tr> </tbody> </table> <p>The context menu is open over the EHC 105 00 module, and a red arrow points to the 'Open Module' option.</p>	Module	Value	CPS	111	CPU	534	EHC	105	ACO	020	DDI	353	DDO	353
Module	Value														
CPS	111														
CPU	534														
EHC	105														
ACO	020														
DDI	353														
DDO	353														
4	Choose Open Module Result: The modul opens with the Parameter Configuration screen														

Parameter Configuration

Overview

This section provides information on the parameters, accessible in the Parameter Configuration Screen.

Parameter Configuration Default Screen

This diagram shows the Parameter Configuration default screen

HI SPEED CNT 5CH	
<input type="checkbox"/> Overview <input checked="" type="checkbox"/> Config	
Parameter Name	Value
MAPPING	WORD (%IW-3X %MW-4X)
INPUTS STARTING ADDRESS	1
INPUTS ENDING ADDRESS	12
OUTPUTS STARTING ADDRESS	1
OUTPUTS ENDING ADDRESS	13
TASK	MAST
<input type="checkbox"/> COUNTERS	
<input type="checkbox"/> COUNTER_1	
<input type="checkbox"/> COUNT INPUT SIGNAL ON NEGATIVE TRANSITION	No
<input type="checkbox"/> USE INPUT 1 FOR COUNTER ENABLE	No
<input type="checkbox"/> WATCHDOG TIMER (0.1S)	0
<input type="checkbox"/> OUTPUT SET POINT 1	0
<input type="checkbox"/> OUTPUT SET POINT 2	0
<input type="checkbox"/> INPUTS_FOR_COUNTER_START/RESTART	
<input type="checkbox"/> LOGIC FUNCTION TO START/RESTART	OR
<input type="checkbox"/> INPUT A	1
<input type="checkbox"/> INPUT B	-
<input type="checkbox"/> INPUT C	-
<input type="checkbox"/> FREEZE_COUNTER_REGISTERS	
<input type="checkbox"/> INPUT D	6
<input type="checkbox"/> INPUT E	-
<input type="checkbox"/> INPUT F	-
<input type="checkbox"/> OUTPUTS	
<input type="checkbox"/> SETPOINT 1 LINKED TO OUTPUT	-
<input type="checkbox"/> INVERT OUTPUT	No
<input type="checkbox"/> SETPOINT 2 LINKED TO OUTPUT	6
<input type="checkbox"/> INVERT OUTPUT	No
<input type="checkbox"/> FINAL SET POINT LINKED TO OUTPUT	1
<input type="checkbox"/> INVERT OUTPUT	No
<input type="checkbox"/> TIMED FINAL SET POINT LINKED TO OUTPUT	-
<input type="checkbox"/> INVERT OUTPUT	No
<input type="checkbox"/> PULSE WIDTH (X 0.02S)	0
<input type="checkbox"/> COUNTER_2	
<input type="checkbox"/> COUNTER_3	
<input type="checkbox"/> COUNTER_4	
<input type="checkbox"/> COUNTER_5	

Local 1.2 : 140

Addressing and Task

This table shows the parameters for addressing and task with its values

Name		Default Value	Options
MAPPING		WORD (%IW-3X%MW-4x)	-
INPUTS STARTING ADDRESS		1	-
INPUTS ENDING ADDRESS		12	-
OUTPUTS STARTING ADDRESS		1	-
OUTPUTS ENDING ADDRESS		13	-
TASK (Grayed if module in other than local)		MAST	FAST AUX0 AUX1 AUX2 AUX3

Counters

This table shows the parameters for the counters with its values

Name		Default Value	Options
COUNTER_1			
COUNT INPUT SIGNAL ON NEGATIVE TRANSITION		No	Yes
USE INPUT 1 FOR COUNTER ENABLE		No	Yes
WATCHDOG TIMER (0.1s)		0	0-255
OUTPUT SET POINT 1		0	0-65535
OUTPUT SET POINT 2		0	0-65535
INPUTS_COUNTER_START/RESTART	LOGIC FUNCTION TO START/RESTART COUNTER	OR	AND
	INPUT A	1	- 1-8
	INPUT B	-	- 1-8
	INPUT C	-	- 1-8
FREEZE_COUNTER_REGISTERS	INPUT D	6	- 1-8
	INPUT E	-	1-8
	INPUT F	-	1-8

Name		Default Value	Options
OUTPUTS	SETPOINT 1 LINKED TO OUTPUT	-	1-8
	● INVERT OUTPUT	No	Yes
	SETPOINT 2 LINKED TO OUTPUT	6	- 1-8
	● INVERT OUTPUT	No	Yes
	FINAL SETPOINT LINKED TO OUTPUT	1	- 1-8
	● INVERT OUTPUT	No	Yes
	TIMED FINAL SETPOINT LINKED TO OUTPUT	-	1-8
	● INVERT OUTPUT	No	Yes
	● PULSE WIDTH (x 0.02s)		0-255
COUNTER_2 COUNTER_3 COUNTER_4 COUNTER_5		See COUNTER_1	

Chapter 10

Configuration Examples

Purpose

This chapter provides configuration examples for the 140 EHC 105 00 high speed counter module.

What Is in This Chapter?

This chapter contains the following sections:

Section	Topic	Page
10.1	Example 1: Event Counter (up, relative)	122
10.2	Example 2: Event Counter (up, absolute)	131
10.3	Example 3: Repetitive Counter (up)	141
10.4	Example 4: Differential Counter (down)	151

Section 10.1

Example 1: Event Counter (up, relative)

Purpose

This section provides an Event Counter (up, relative) as an example for the configuration of the 140 EHC 105 00.

What Is in This Section?

This section contains the following topics:

Topic	Page
Prerequisites and Software Configuration	123
Hardware Setup and Wiring	125
Schematic	127
Parameter Configuration Screen	128
Operation and Timing	129

Prerequisites and Software Configuration

Overview

This section provides the prerequisites for the configuration example 1: Event Counter (up, relative) and the configuration method (I/O Configuration and Parameter Configuration) related to each item.

NOTE: The controller must be stopped before configuring the 140 EHC 105 00

I/O Configuration

This table shows prerequisites related to I/O configuration.

Prerequisites of the Example		I/O configuration			
		Address	Assignment	Value	Datatype
counter_1	Event counter with parallel Set Point activation	4x (e.q 400100)	OCW 1	1010	Hex
	counter_1 counts up				
	Values for output Set Points are relative (refers to all counters)				
	if communication is lost the counter outputs are set to "0" (refers to all counters)				
	Final Set Point: E/S1	4x+3 (e.q 400103)		30 e.q	Long Decimal

Parameter Configuration

This table shows prerequisites related to Parameter configuration.

Prerequisites of the Example		Parameter Configuration
=Parameter		Value
counter_1		
COUNT INPUT SIGNAL ON NEGATIVE TRANSITION		yes
USE INPUT 1 FOR COUNTER ENABLE		yes
WATCHDOG TIMER (0.1s)		0
OUTPUT SET POINT 1		11
OUTPUT SET POINT 2		5
INPUTS_COUNTER_START/ RESTART	LOGIC FUNCTION TO START/RESTART COUNTER	OR
	INPUT A	6
FREEZE_COUNTER_REGISTERS	INPUT D	8
OUTPUTS	SETPOINT 1 LINKED TO OUTPUT	1
	SETPOINT 2 LINKED TO OUTPUT	2
	FINAL SETPOINT LINKED TO OUTPUT	3
	TIMED FINAL SETPOINT LINKED TO OUTPUT	4
	● INVERT OUTPUT	No
	● PULSE WIDTH (x 0.02s)	20

NOTE: All settable values including those of the table are in the *Parameter Configuration Screen*, [page 128](#) of this example.

Hardware Setup and Wiring

Overview

This section provides a procedure to mount and field wire the 140 EHC 105 00 module within a Quantum system.

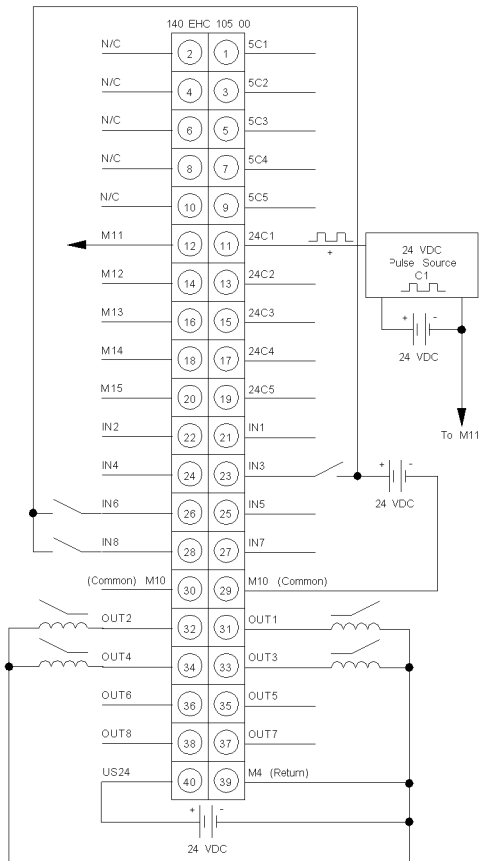
Mounting

This table shows the procedure to mount the 140 EHC 105 00 module

Step	Action
1	Mount the 140 EHC 105 00 in the specified backplane (local, RIO or DIO)
2	Install the module terminal strip
3	Connect an external 24 VDC supply voltage as shown in the wiring diagram: pin 40 (+) pin 39 (-)
4	Connect the pulse input source to channel 1 (pin 11),

Wiring

This diagram shows the wiring of the example configuration of the 140 EHC 105 00



NOTE: The tightening torque must be between 0.5 Nm and 0.8 Nm.

NOTICE

DESTRUCTION OF ADAPTER

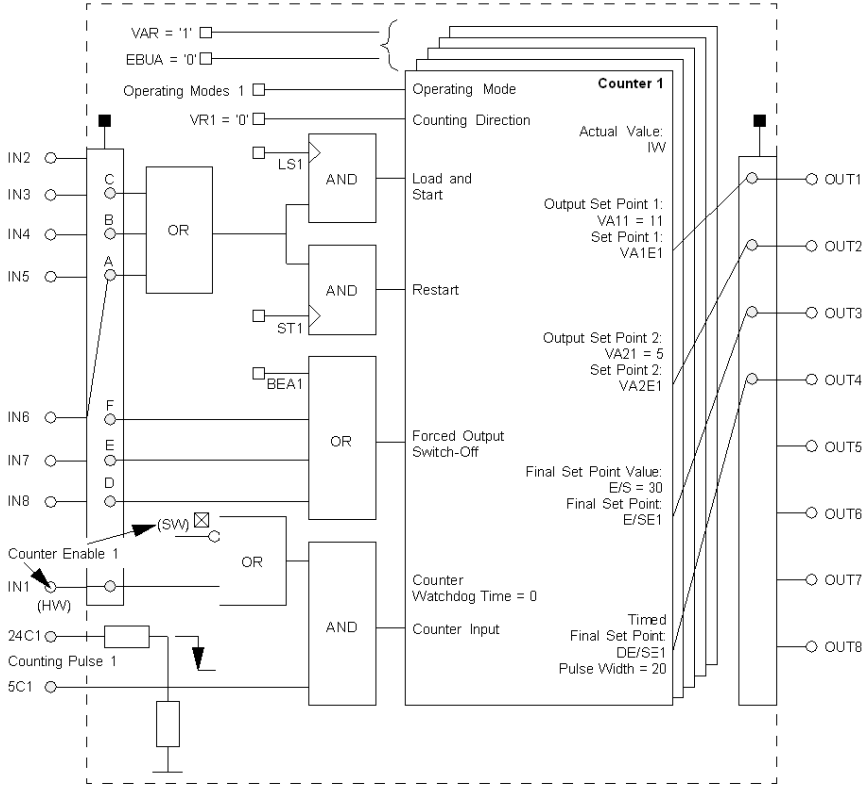
- Before tightening the locknut to the torque 0.50...0.80 Nm, be sure to properly position the right-angle F adapter connector.
- During tightening, be sure to maintain the connector securely.
- Do not tighten the right-angle F adapter beyond the specified torque.

Failure to follow these instructions can result in equipment damage.

Schematic

Overview

This diagram shows the schematic of the example configuration.



⚠ CAUTION

INVALID CONFIGURATION

Do not use outputs OUT1...OUT4 with other counters; as such multiple usage is prohibited.
Failure to follow these instructions can result in injury or equipment damage.

Parameter Configuration Screen

Parameter Configuration Screen

This diagram shows the Parameter Configuration Screen with the parameters set for the example.

HI SPEED CNT 5CH

Overview
 Config

Parameter Name	Value
--- MAPPING	WORD (%IW-3X %MW-4X)
--- INPUTS STARTING ADDRESS	1
--- INPUTS ENDING ADDRESS	12
--- OUTPUTS STARTING ADDRESS	1
--- OUTPUTS ENDING ADDRESS	13
--- TASK	MAST
<input type="checkbox"/> --- COUNTERS	
<input type="checkbox"/> --- COUNTER_1	
--- COUNT INPUT SIGNAL ON NEGATIVE TRANSITION	Yes
--- USE INPUT 1 FOR COUNTER ENABLE	Yes
--- WATCHDOG TIMER (0.1S)	0
--- OUTPUT SET POINT 1	11
--- OUTPUT SET POINT 2	5
<input type="checkbox"/> --- INPUTS_FOR_COUNTER_START/RESTART	
--- LOGIC FUNCTION TO START/RESTART COUNTER	OR
--- INPUT A	6
--- INPUT B	-
--- INPUT C	-
<input type="checkbox"/> --- FREEZE_COUNTER_REGISTERS	
--- INPUT D	8
--- INPUT E	-
--- INPUT F	-
<input type="checkbox"/> --- OUTPUTS	
<input type="checkbox"/> --- SETPOINT 1 LINKED TO OUTPUT	1
--- INVERT OUTPUT	No
<input type="checkbox"/> --- SETPOINT 2 LINKED TO OUTPUT	2
--- INVERT OUTPUT	No
<input type="checkbox"/> --- FINAL SET POINT LINKED TO OUTPUT	3
--- INVERT OUTPUT	No
<input type="checkbox"/> --- TIMED FINAL SET POINT LINKED TO OUTPUT	4
--- INVERT OUTPUT	No
--- PULSE WIDTH (X 0.02S)	20
<input checked="" type="checkbox"/> --- COUNTER_2	
<input checked="" type="checkbox"/> --- COUNTER_3	
<input checked="" type="checkbox"/> --- COUNTER_4	
<input checked="" type="checkbox"/> --- COUNTER_5	

Local Quant...
 12 : 140 EH...

Operation and Timing

Start Counter_1

This table shows the procedure to start Counter_1

Step	Action	Effect
1	To start the counter, activate input 6 (IN6="1")	
2	Enter 1110 Hex in 4x-Register (e.q. 400100) Result: LS1 (Bit 8 in OCW1) is set to "1"	The actual value of counter_1 (IW1) is set to "0" The initial levels of Set Points are transferred to the related outputs: VA1E1->OUT1="1" VA2E1->OUT2="1" E/SE1 ->OUT3="1" DE/SE1 ->OUT4="0"
3	To enable counter_1, activate input 1 (IN1="1") Result: counter_1 counts the pulses at counter input 24C1	Output values, depend on the actual value of counter_1: For IW1=19 (30-11)->OUT1="0" For IW1=25 (30-5) ->OUT2="0" For IW1=30->OUT3="0" For IW1=30->OUT4="1" (Timed Final Set Point for 400 ms)

Switch off the outputs

This table shows the procedure to switch off the outputs, before reaching the specified Set Points

Step	Action	Effect
1	To switch off the outputs (OUT1-OUT4) there are two possibilities: 1. Possibility: Activate input 8 (IN8="1") 2. Possibility: Enter 1410 Hex in 4x-Register (e.q. 400100); Result: BEA1=1	OUT1->"0" OUT2->"0" OUT3->"0" OUT4->"0"

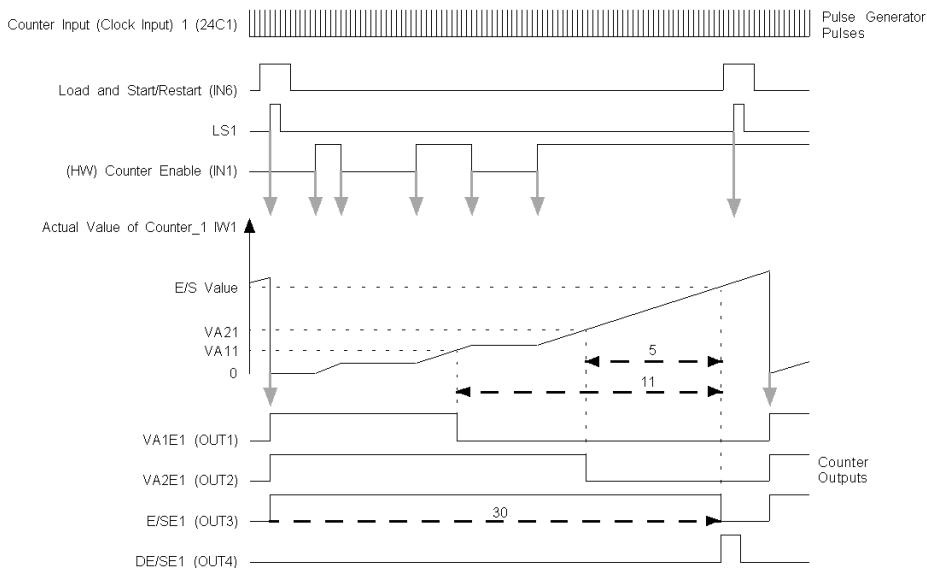
Restart Counter_1

This table shows the procedure to restart Counter_1. This however is only possible, if the Final Set Point value (here 30) has not yet been reached.

Step	Action	Effect
1	Switch off the outputs as seen in the previous table	
2	To restart the counter, activate input 6 (IN6="1")	The actual counting value will be set to "0"
3	Enter 1210 Hex in 4x-Register (e.q. 400100) Result: ST1 (Bit 9 in OCW1) is set to "1"	The output values will be set to "0"
4	To reenale counter_1, activate input 1 (IN1="1")	The Set Points (apart from DE/SE1) will be set to "1"

Timing Diagram

This diagram shows the timing of the example configuration



NOTE: If pulses continue at counter input 24C1, after reaching the Final Set Point value, the EHC 105 keeps on counting. The result is stored in two successive input registers as a 32-bit value (see *3x-Register assignment, page 97*).

If the counter's operating mode, counting direction, switch-off behavior, or type of Set Point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

Section 10.2

Example 2: Event Counter (up, absolute)

Purpose

This section provides an Event Counter (up, absolute) as an example for the configuration of the 140 EHC 105 00.

What Is in This Section?

This section contains the following topics:

Topic	Page
Prerequisites and Software Configuration	132
Hardware Setup and Wiring	134
Schematic	137
Parameter Configuration Screen	138
Operation and Timing	139

Prerequisites and Software Configuration

Overview

This section provides the prerequisites for the configuration example 2: Event Counter (up, absolute) and the configuration method (I/O Configuration and Parameter Configuration) related to each item.

NOTE: The controller must be stopped before configuring the 140 EHC 105 00

I/O Configuration

This table shows prerequisites related to I/O configuration.

Prerequisites of the Example		I/O configuration			
		Address	Assignment	Value	Datatype
all counters	Values for output Set Points are absolute	4x (e.q 400100)	OCW 1	0000	Hex
	if communication is lost the counter outputs are set to "0"				
counter_4	Event counter with timed "on" outputs; the pulse width setting refers to all related outputs	4x+2 (e.q 400102)	OCW 3	00A0	Hex
	counter_4 counts up				
	Final Set Point: E/S4	4x+9 (e.q 400109)		30 e.q	Long Decimal

Parameter Configuration

This table shows prerequisites related to Parameter configuration.

Prerequisites of the Example =Parameter		Parameter Configuration Value
counter_4		
COUNT INPUT SIGNAL ON NEGATIVE TRANSITION		yes
USE INPUT 4 FOR COUNTER ENABLE		yes
WATCHDOG TIMER (0.1s)		0
OUTPUT SET POINT 1		5
OUTPUT SET POINT 2		11
INPUTS_COUNTER_START/ RESTART	LOGIC FUNCTION TO START/RESTART COUNTER	OR
	INPUT A	7
FREEZE_COUNTER_REGISTERS	INPUT D	8
OUTPUTS	SETPOINT 1 LINKED TO OUTPUT	5
	SETPOINT 2 LINKED TO OUTPUT	6
	FINAL SETPOINT LINKED TO OUTPUT	7
	TIMED FINAL SETPOINT LINKED TO OUTPUT	8
	● INVERT OUTPUT	No
	● PULSE WIDTH (x 0.02s)	100

NOTE: All settable values including those of the table are in the *Parameter Configuration Screen*, [page 148](#) of this example.

Hardware Setup and Wiring

Overview

This section provides a procedure to mount and field wire the 140 EHC 105 00 module within a Quantum system.

Mounting

This table shows the procedure to mount the 140 EHC 105 00 module

Step	Action
1	Mount the 140 EHC 105 00 in the specified backplane (local, RIO or DIO)
2	Install the module terminal strip
3	Connect an external 24 VDC supply voltage as shown in the wiring diagram: pin 40 (+) pin 39 (-)
4	Connect the pulse input source to channel 4 (pin 17)

NOTE: The tightening torque must be between 0.5 Nm and 0.8 Nm.

NOTICE

DESTRUCTION OF ADAPTER

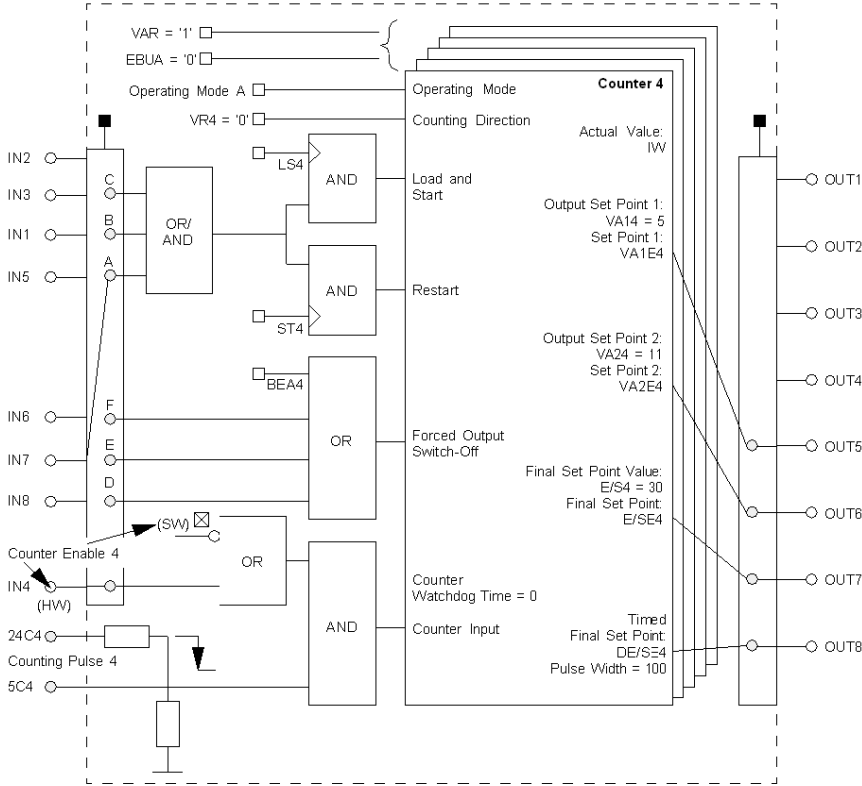
- Before tightening the locknut to the torque 0.50...0.80 Nm, be sure to properly position the right-angle F adapter connector.
- During tightening, be sure to maintain the connector securely.
- Do not tighten the right-angle F adapter beyond the specified torque.

Failure to follow these instructions can result in equipment damage.

Schematic

Overview

This diagram shows the schematic of the example configuration.



⚠ CAUTION

INVALID CONFIGURATION

Do not use outputs OUT1...OUT4 with other counters; as such multiple usage is prohibited.

Failure to follow these instructions can result in injury or equipment damage.

Parameter Configuration Screen

Parameter Configuration Screen

This diagram shows the Parameter Configuration Screen with the parameters set for the example.

HIsPEED CNT 5CH

Overview

Config

Parameter Name	Value
--- MAPPING	WORD (%IW-3X %MW-4X)
--- INPUTS STARTING ADDRESS	1
--- INPUTS ENDING ADDRESS	12
--- OUTPUTS STARTING ADDRESS	1
--- OUTPUTS ENDING ADDRESS	13
--- TASK	MAST
[-] COUNTERS	
+ COUNTER_1	
+ COUNTER_2	
+ COUNTER_3	
[-] COUNTER_4	
--- COUNT INPUT SIGNAL ON NEGATIVE TRANSITION	Yes
--- USE INPUT 4 FOR COUNTER ENABLE	Yes
--- WATCHDOG TIMER (0.1S)	0
--- OUTPUT SET POINT 1	5
--- OUTPUT SET POINT 2	11
[-] INPUTS_FOR_COUNTER_START/RESTART	
--- LOGIC FUNCTION TO START/RESTART COUNTER	OR
--- INPUT A	7
--- INPUT B	-
--- INPUT C	-
[-] FREEZE_COUNTER_REGISTERS	
--- INPUT D	8
--- INPUT E	-
--- INPUT F	-
[-] OUTPUTS	
[-] SETPOINT 1 LINKED TO OUTPUT	5
--- INVERT OUTPUT	No
[-] SETPOINT 2 LINKED TO OUTPUT	6
--- INVERT OUTPUT	No
[-] FINAL SET POINT LINKED TO OUTPUT	7
--- INVERT OUTPUT	No
[-] TIMED FINAL SET POINT LINKED TO OUTPUT	8
--- INVERT OUTPUT	No
--- PULSE WIDTH (X 0.02S)	100
+ COUNTER_5	

Local Quant...
↑ 1.2 : 140.EH..

Operation and Timing

Start Counter_4

This table shows the procedure to start Counter_4

Step	Action	Effect
1	To start the counter, activate input 7 (IN7="1")	
2	Enter 00A1 Hex in 4x-Register (e.q. 400102) Result: LS4 (Bit 0 in OCW3) is set to "1"	The actual value of counter_4 (IW4) is set to "0" VA1E4="1" VA2E4="1" E/SE4 ="1" Outputs are set to "0": OUT5="0" OUT6="0" OUT7="0" DE/SE4 ->OUT8="0"
3	To enable counter_4, activate input 4 (IN4="1") Result: counter_4 counts the pulses at counter input 24C4	If the actual value of counter_4 equals the specified Set Point value, the related output will switch on for 2 seconds: For IW4=5->OUT5="1" For IW4=11->OUT6="1" For IW4=30->OUT7="1" and OUT8="1"

Switch off the outputs

This table shows the procedure to switch off the outputs, before reaching the specified Set Points

Step	Action	Effect
1	To switch off the outputs (OUT5-OUT8) there are two possibilities: 1. Possibility: Activate input 7 (IN7="1") 2. Possibility: Enter 00A4 Hex in 4x-Register (e.q. 400100); Result: BEA4=1	OUT5->"0" OUT6->"0" OUT7->"0" OUT8->"0"

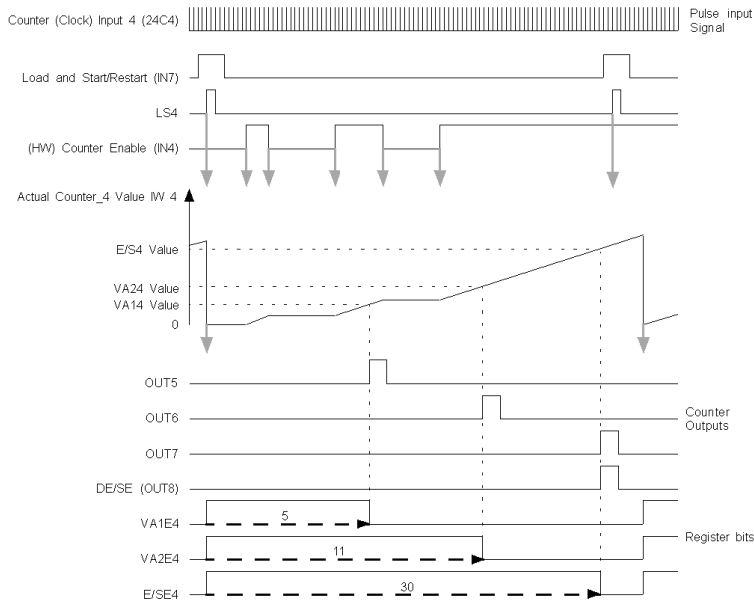
Restart Counter_4

This table shows the procedure to restart Counter_4. This however is only possible, if the Final Set Point value (here 30) has not yet been reached.

Step	Action	Effect
1	Switch off the outputs as seen in the previous table	
2	To restart the counter, activate input 7 (IN7="1")	The actual counting value will be set to "0" The output values will be set to "0"
3	Enter 00A1 Hex in 4x-Register (e.g. 400102) Result: ST4 (Bit 1 in OCW3) is set to "1"	
4	To reenale counter_4, activate input 4 (IN4="1")	The register values (Set Points) will be set to "1"

Timing Diagram

This diagram shows the timing of the example configuration



NOTE: If pulses continue at counter input 24C4, after reaching the Final Set Point value (here 30), the EHC 105 keeps on counting. The result is stored in two successive input registers as a 32-bit value (see *3x-Register assignment, page 97*).

If the counter's operating mode, counting direction, switch-off behavior, or type of Set Point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

Section 10.3

Example 3: Repetitive Counter (up)

Purpose

This section provides an Repetitive Counter (up) as an example for the configuration of the 140 EHC 105 00.

What Is in This Section?

This section contains the following topics:

Topic	Page
Prerequisites and Software Configuration	142
Hardware Setup and Wiring	144
Schematic	147
Parameter Configuration Screen	148
Operation and Timing	149

Prerequisites and Software Configuration

Overview

This section provides the prerequisites for the configuration example 3: Repetitive Counter (up, relative) and the configuration method (I/O Configuration and Parameter Configuration) related to each item.

NOTE: The controller must be stopped before configuring the 140 EHC 105 00

I/O Configuration

This table shows prerequisites related to I/O configuration.

Prerequisites of the Example		I/O configuration			
		Address	Assignment	Value	Datatype
all counters	Values for output Set Points are relative	4x (e.q 400100)	OCW 2	0010	Hex
	if communication is lost the counter outputs are set to "0"				
counter_2	Repetitive counter	4x+1 (e.q 400101)	OCW 2	0050	Hex
	counter_2 counts up				
	Final Set Point: E/S2	4x+5 (e.q 400105)		30 e.q	Long Decimal

Parameter Configuration

This table shows prerequisites related to Parameter configuration.

Prerequisites of the Example =Parameter		Parameter Configuration Value
counter_2		
COUNT INPUT SIGNAL ON NEGATIVE TRANSITION		yes
USE INPUT 2 FOR COUNTER ENABLE		No
WATCHDOG TIMER (0.1s)		0
OUTPUT SET POINT 1		11
OUTPUT SET POINT 2		5
INPUTS_COUNTER_START/RESTART	LOGIC FUNCTION TO START/RESTART COUNTER	OR
	INPUT A	2
FREEZE_COUNTER_REGISTERS	INPUT D	8
OUTPUTS	SETPOINT 1 LINKED TO OUTPUT	1
	SETPOINT 2 LINKED TO OUTPUT	2
	FINAL SETPOINT LINKED TO OUTPUT	3
	TIMED FINAL SETPOINT LINKED TO OUTPUT	4
	● INVERT OUTPUT	No
	● PULSE WIDTH (x 0.02s)	20

NOTE: All settable values including those of the table are in the *Parameter Configuration Screen*, [page 138](#) of this example.

Hardware Setup and Wiring

Overview

This section provides a procedure to mount and field wire the 140 EHC 105 00 module within a Quantum system.

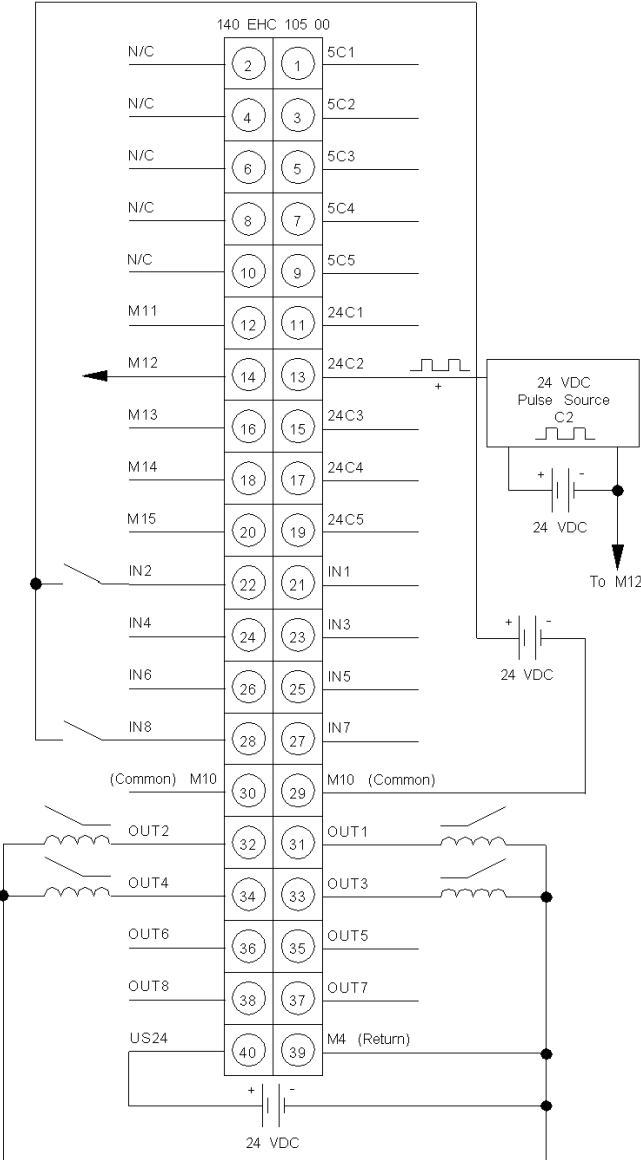
Mounting

This table shows the procedure to mount the 140 EHC 105 00 module

Step	Action
1	Mount the 140 EHC 105 00 in the specified backplane (local, RIO or DIO)
2	Install the module terminal strip
3	Connect an external 24 VDC supply voltage as shown in the wiring diagram: pin 40 (+) pin 39 (-)
4	Connect the pulse input source to channel 2 (pin 13)

Wiring

This diagram shows the wiring of the example configuration of the 140 EHC 105 00



NOTE: The tightening torque must be between 0.5 Nm and 0.8 Nm.

NOTICE

DESTRUCTION OF ADAPTER

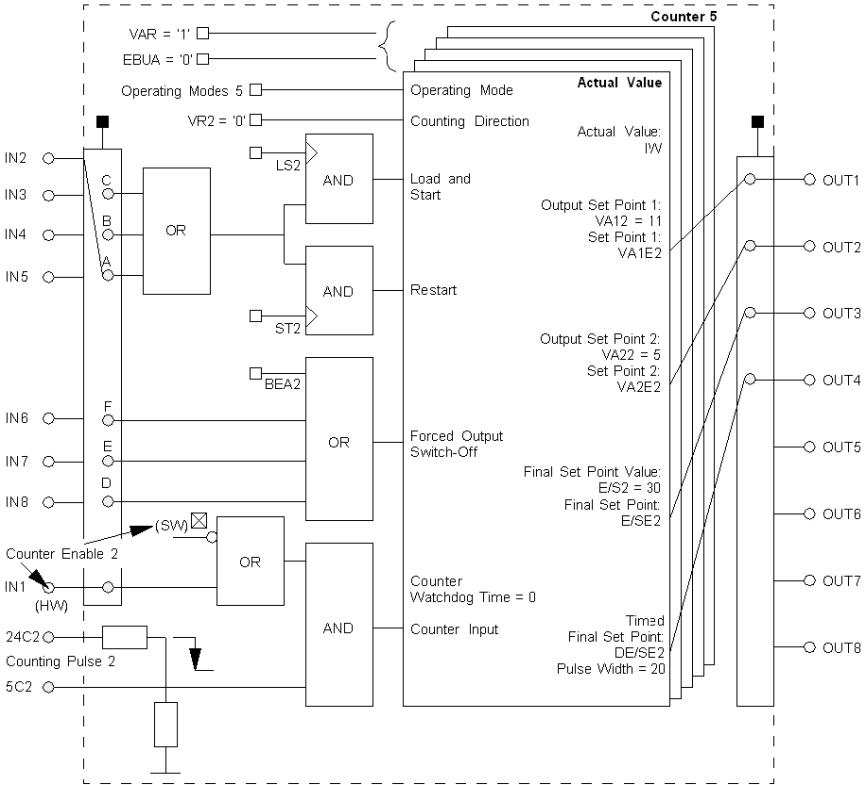
- Before tightening the locknut to the torque 0.50...0.80 Nm, be sure to properly position the right-angle F adapter connector.
- During tightening, be sure to maintain the connector securely.
- Do not tighten the right-angle F adapter beyond the specified torque.

Failure to follow these instructions can result in equipment damage.

Schematic

Overview

This diagram shows the schematic of the example configuration.



⚠ CAUTION

INVALID CONFIGURATION

Do not use outputs OUT1...OUT4 with other counters; as such multiple usage is prohibited.
Failure to follow these instructions can result in injury or equipment damage.

Parameter Configuration Screen

Parameter Configuration Screen

This diagram shows the Parameter Configuration Screen with the parameters set for the example.

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Overview

Config

Parameter Name	Value
--- MAPPING	WORD (%IW-3X %MW-4X)
INPUTS STARTING ADDRESS	1
INPUTS ENDING ADDRESS	12
OUTPUTS STARTING ADDRESS	1
OUTPUTS ENDING ADDRESS	13
TASK	MAST
[-] COUNTERS	
[+] COUNTER_1	
[-] COUNTER_2	
COUNT INPUT SIGNAL ON NEGATIVE TRANSITION	Yes
USE INPUT 4 FOR COUNTER ENABLE	No
WATCHDOG TIMER (0.1S)	0
OUTPUT SET POINT 1	11
OUTPUT SET POINT 2	5
[-] INPUTS_FOR_COUNTER_START/RESTART	
LOGIC FUNCTION TO START/RESTART COUNTER	OR
INPUT A	2
INPUT B	-
INPUT C	-
[-] FREEZE_COUNTER_REGISTERS	
INPUT D	8
INPUT E	-
INPUT F	-
[-] OUTPUTS	
[-] SETPOINT 1 LINKED TO OUTPUT	1
INVERT OUTPUT	No
[-] SETPOINT 2 LINKED TO OUTPUT	2
INVERT OUTPUT	No
[-] FINAL SET POINT LINKED TO OUTPUT	3
INVERT OUTPUT	No
[-] TIMED FINAL SET POINT LINKED TO OUTPUT	4
INVERT OUTPUT	No
PULSE WIDTH (X 0.02S)	20
[+] COUNTER_3	
[+] COUNTER_4	
[+] COUNTER_5	

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Operation and Timing

Overview

NOTE: In this configuration the counter input is inherently enabled, as there has not been assigned a discrete input.

Start Counter_2

This table shows the procedure to start Counter_2

Step	Action	Effect
1	To start the counter, activate input 2 (IN2="1")	
2	Enter 0051 Hex in 4x-Register (e.q. 400101) Result: LS2 (Bit 0 in OCW1) is set to "1"	The actual value of counter_2 (IW2) is set to "0" The initial levels of Set Points are transferred to the related outputs: VA1E2->OUT1="1" VA2E2->OUT2="0" E/SE2 ->OUT3="0" DE/SE2 ->OUT4="0"

Output values

This table shows the output values, depending on the actual value of the counter_2

Actual value of counter	Output
For IW2=19 (30-11)	OUT1="0" OUT2="1"
For IW2=25 (30-5)	OUT2="0" OUT3="1"
For IW2=30	OUT1="1" OUT3="0" OUT4="1" (Timed Final Set Point for 400 ms)

Switch off the outputs

This table shows the procedure to switch off the outputs, before reaching the specified Set Points

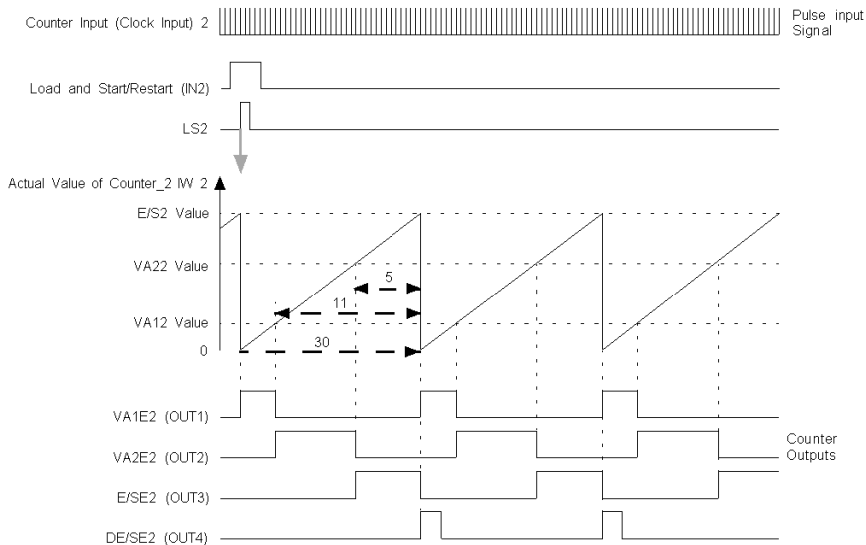
Step	Action	Effect
1	To switch off the outputs (OUT1-OUT3) there are two possibilities: 1. Possibility: Activate input 8 (IN8="1") 2. Possibility: Enter 0054 Hex in 4x-Register (e.q. 400101); Result: BEA2=1	OUT1->"0" OUT2->"0" OUT3->"0"

Restart counter_2

NOTE: Restart of counter_2 in this configuration/mode is not possible

Timing Diagram

This diagram shows the timing of the example configuration



NOTE: If the counter's operating mode, counting direction, switch-off behavior, or type of Set Point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

Section 10.4

Example 4: Differential Counter (down)

Purpose

This section provides an Differential Counter (down) as an example for the configuration of the 140 EHC 105 00.

What Is in This Section?

This section contains the following topics:

Topic	Page
Prerequisites and Software Configuration	152
Hardware Setup and Wiring	154
Schematic	157
Parameter Configuration Screen	158
Operation and Timing	159

Prerequisites and Software Configuration

Overview

This section provides the prerequisites for the configuration example 4: Differential Counter (down, relative) and the configuration method (I/O Configuration and Parameter Configuration) related to each item.

NOTE: The controller must be stopped before configuring the 140 EHC 105 00

Principle

A differential counter uses two channels. In this example the channels are represented by counter 3 and counter 4. Counter 3 serves as master and its configuration also applies to counter 4.

The parameters specified for counter 4, will be ignored apart from:

- COUNT INPUT SIGNAL ON NEGATIVE TRANSITION
- USE INPUT 4 FOR COUNTER ENABLE

The pulses for counter 3 count up and the pulses for counter 4 count down. The counting results in the actual difference value .

I/O Configuration

This table shows prerequisites related to I/O configuration.

Prerequisites of the Example		I/O configuration			
		Address	Assignment	Value	Datatype
all counters	Values for output Set Points are relative	4x (e.q 400100)	OCW 1	0010	Hex
	if communication is lost the counter outputs are set to "0"				
counter_3	Differential counter with parallel Set Point activation	4x+1 (e.q 400101)	OCW 2	3800	Hex
	counter_3 counts down				
	Final Set Point: E/S3	4x+7 (e.q 400107)		30 e.q	Long Decimal

Parameter Configuration

This table shows prerequisites related to Parameter configuration.

Prerequisites of the Example =Parameter		Parameter Configuration Value
counter_3		
COUNT INPUT SIGNAL ON NEGATIVE TRANSITION		yes
USE INPUT 3 FOR COUNTER ENABLE		No
WATCHDOG TIMER (0.1s)		0
OUTPUT SET POINT 1		11
OUTPUT SET POINT 2		5
INPUTS_COUNTER_START/RESTART	LOGIC FUNCTION TO START/RESTART COUNTER	OR
	INPUT A	-
FREEZE_COUNTER_REGISTERS	INPUT D	-
OUTPUTS	SETPOINT 1 LINKED TO OUTPUT	1
	SETPOINT 2 LINKED TO OUTPUT	2
	FINAL SETPOINT LINKED TO OUTPUT	3
	TIMED FINAL SETPOINT LINKED TO OUTPUT	4
	● INVERT OUTPUT	No
	● PULSE WIDTH (x 0.02s)	20

NOTE: All settable values including those of the table are in the *Parameter Configuration Screen*, [page 158](#) of this example.

Hardware Setup and Wiring

Overview

This section provides a procedure to mount and field wire the 140 EHC 105 00 module within a Quantum system.

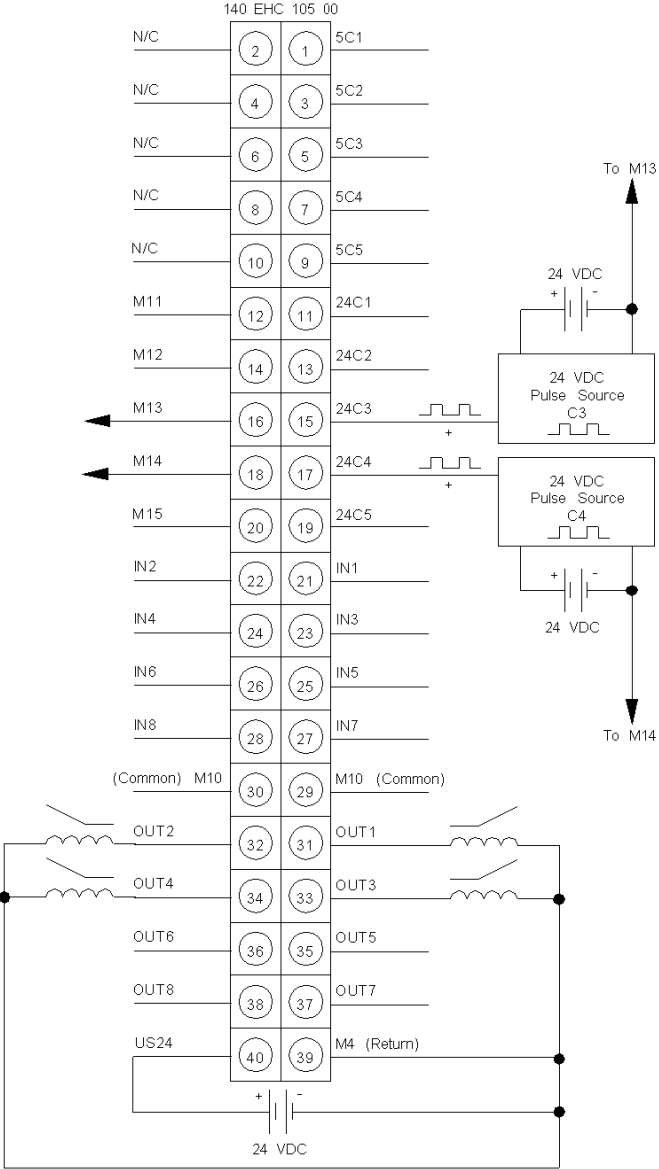
Mounting

This table shows the procedure to mount the 140 EHC 105 00 module

Step	Action
1	Mount the 140 EHC 105 00 in the specified backplane (local, RIO or DIO)
2	Install the module terminal strip
3	Connect an external 24 VDC supply voltage as shown in the wiring diagram: pin 40 (+) pin 39 (-)
4	Connect the first pulse input source to channel 3 (pin 15)
5	Connect the second pulse input source to channel 4 (pin 17)

Wiring

This diagram shows the wiring of the example configuration of the 140 EHC 105 00



NOTE: The tightening torque must be between 0.5 Nm and 0.8 Nm.

NOTICE

DESTRUCTION OF ADAPTER

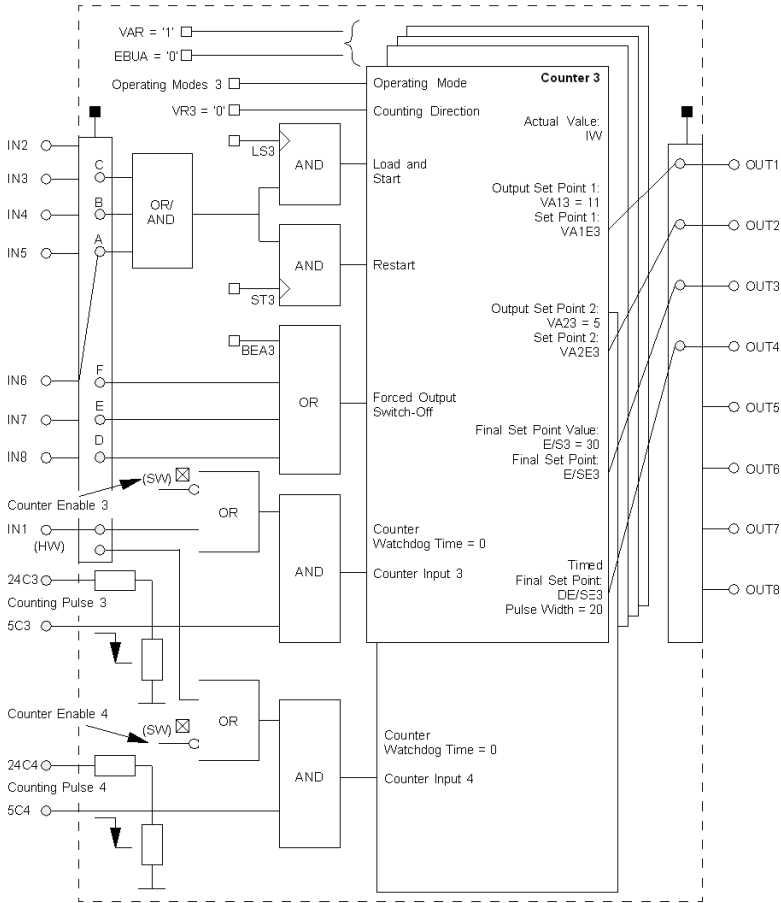
- Before tightening the locknut to the torque 0.50...0.80 Nm, be sure to properly position the right-angle F adapter connector.
- During tightening, be sure to maintain the connector securely.
- Do not tighten the right-angle F adapter beyond the specified torque.

Failure to follow these instructions can result in equipment damage.

Schematic

Overview

This diagram shows the schematic of the example configuration.



⚠ CAUTION

INVALID CONFIGURATION

Do not use outputs OUT1...OUT4 with other counters; as such multiple usage is prohibited.

Failure to follow these instructions can result in injury or equipment damage.

Parameter Configuration Screen

Parameter Configuration Screen

This diagram shows the Parameter Configuration Screen with the parameters set for the example.

HI SPEED CNT 5CH

Overview
 Config

Parameter Name	Value
MAPPING	WORD (%IW-3X %MW-4X)
INPUTS STARTING ADDRESS	1
INPUTS ENDING ADDRESS	12
OUTPUTS STARTING ADDRESS	1
OUTPUTS ENDING ADDRESS	13
TASK	MAST
[-] COUNTERS	
+ COUNTER_1	
+ COUNTER_2	
[-] COUNTER_3	
COUNT INPUT SIGNAL ON NEGATIVE TRANSITION	Yes
USE INPUT 3 FOR COUNTER ENABLE	No
WATCHDOG TIMER (0.1S)	0
OUTPUT SET POINT 1	11
OUTPUT SET POINT 2	5
[-] INPUTS_FOR_COUNTER_START/RESTART	
LOGIC FUNCTION TO START/RESTART	OR
INPUT A	-
INPUT B	-
INPUT C	-
[-] FREEZE_COUNTER_REGISTERS	
INPUT D	-
INPUT E	-
INPUT F	-
[-] OUTPUTS	
[-] SETPOINT 1 LINKED TO OUTPUT	1
INVERT OUTPUT	No
SETPOINT 2 LINKED TO OUTPUT	2
INVERT OUTPUT	No
[-] FINAL SET POINT LINKED TO OUTPUT	3
INVERT OUTPUT	No
TIMED FINAL SET POINT LINKED TO OUTPUT	4
INVERT OUTPUT	No
PULSE WIDTH (X 0.02S)	20
+ COUNTER_4	
+ COUNTER_5	

Local
 1.2 : 140

Operation and Timing

Overview

NOTE: In this configuration the counter input is inherently enabled, as there has not been assigned a discrete input.

Start Differential counter

This table shows the procedure to start Differential counter

Step	Action	Effect
1	Enter 3900 Hex in 4x-Register (e.g. 400101) Result: LS3 (Bit 8 in OCW2) is set to "1"	The actual difference value is set to "30" The initial levels of Set Points for counter 3 are transferred to the related outputs: VA1E3->OUT1="1" VA2E3->OUT2="1" E/SE3 ->OUT3="1" DE/SE3 ->OUT4="0"

Output values

This table shows the output values, depending on the actual difference value of both counters

Actual difference value	Output
11	OUT1="0"
5	OUT2="0"
0	OUT3="0" OUT4="1" (Timed Final Set Point for 400 ms)

Switch off the outputs

This table shows the procedure to switch off the outputs, before reaching the specified Set Points

Step	Action	Effect
1	To switch off the outputs (OUT1-OUT4) there are two possibilities: 1. Possibility: Activate input 8 (IN8="1") 2. Possibility: Enter 3C00 Hex in 4x-Register (e.g. 400101); Result: BEA3=1	OUT1->"0" OUT2->"0" OUT3->"0" OUT3->"0"

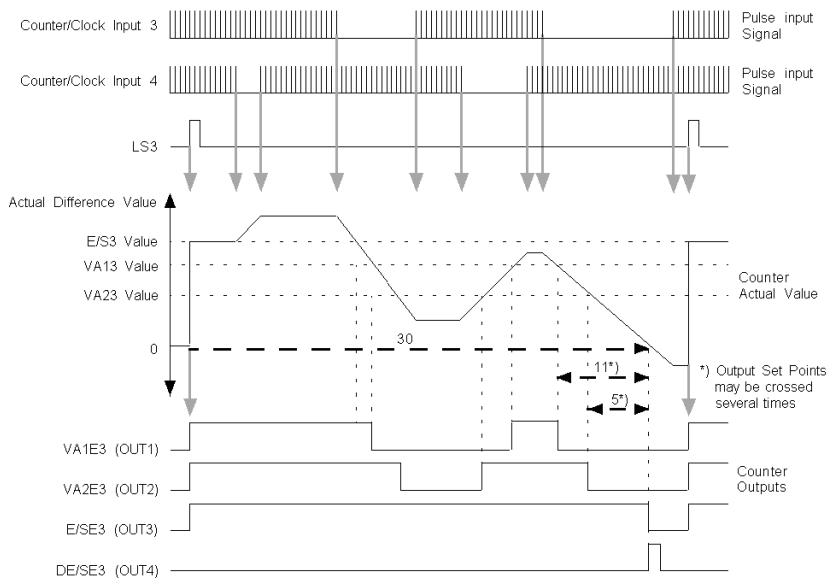
Restart Differential Counter

This table shows the procedure to restart the differential counter. This however is only possible, if the Final Set Point value (here 30) has not yet been reached.

Step	Action	Effect
1	Switch off the outputs as seen in the previous table	
2	Enter 3A00 Hex in 4x-Register (e.q. 400101) Result: ST3 (Bit 10 in OCW2) is set to "1"	The actual difference value will be set to "30" The outputs OUT1-OUT3 will be set to "1" The Set Points (except DE/SE3) will be set to "1"

Timing Diagram

This diagram shows the timing of the example configuration



NOTE: If pulses continue at counter input 24C3 or 24C4, after reaching the Final Set Point value (here 30), the EHC 105 keeps on counting. The result is stored in two successive input registers as a 32-bit value (see *3x-Register assignment, page 97*).

If the counter's operating mode, counting direction, switch-off behavior, or type of Set Point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.



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